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The goal of this project is to develop advanced control strategies that enable realization of highly efficient, modular medium-voltage dc-ac and dc-dc energy conversion systems by development of new control strategies that improve the operational characteristics of the dc-ac and dc-dc MMC with regard to minimization of the capacitor voltage ripple and circulating currents, thereby improving the converter's efficiency and power density.

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ABSTRACT

The modular multilevel converter (MMC) is increasingly becoming popular for multi-MW drive systems. One of the main technical challenges associated with the operation of MMC for adjustable-speed drives is the large magnitude of submodule (SM) capacitor voltage ripple under constant-torque low-speed operation. This project proposes two new control strategies to reduce the magnitude of the SM capacitor voltage ripple in the MMC-based adjustable-speed drive systems under constant-torque low-speed operation. The proposed control strategies are based on injecting a square-wave common-mode voltage at the ac-side and a circulating current within the phase-legs to attenuate the low-frequency components of the SM capacitor voltages. The frequency spectrum of the injected circulating current consists of components in the vicinity of either the common-mode frequency or the common-mode frequency and third harmonic of the common-mode frequency. This report also provides (i) a theoretical comparison of the proposed control strategies with the existing ones, (ii) a controller design methodology to systematically determine the controller gains of the proposed control strategies, and (iii) a theoretical proof of stability of the proposed control strategies and their design methodology based on Lyapunov analysis of singularly perturbed non-linear non-autonomous systems. A set of experimental results for various case studies on a laboratory-scale prototype are provided to support the theoretical proof of stability of the proposed control strategies and their design methodology, and to show the superior performance of the proposed strategies over the existing strategy. The DC-DC Modular Multilevel Converter (MMC), which has originated from the AC-DC MMC circuit topology, is an attractive converter topology for interconnection of medium-/high-voltage DC grids. The objective of the proposed research is to address the technical challenges associated with the operation and control of the DC-DC MMC. To this end, first, a phasor-domain mathematical model of the DC-DC MMC is proposed to determine the AC and DC components of the arm current, phase current, and Sub-Module (SM) capacitor voltage ripple under steady state. A design procedure for the DC-DC MMC based on the proposed mathematical model is developed to achieve high efficiency and to reduce the size of components. The proposed design procedure includes sizing of the arm inductor, submodule capacitor, and phase filtering inductor along with the selection of AC operating frequency of the converter. The accuracy of the developed model and the effectiveness of the design approach are validated based on the simulation studies

in the PSCAD/EMTDC software environment.

Proper operation of the DC-DC MMC necessitates injection of an AC circulating current to maintain its SM capacitor voltages balanced. The AC circulating current, however, needs to be minimized for efficiency improvement. To regulate the active AC power of each arm and to maintain the SM capacitor voltages balanced, two closed-loop control strategies, one based on an Model-based Close-loop Controller (MCC) and the other based on a Push-Pull Closed-loop Controller (PCC) are proposed to control the DC-DC MMC. Both control strategies are capable of simultaneously regulating the output DC-link voltage, maintaining the SM capacitor voltages balanced and minimizing the AC circulating current. The proposed control strategies employ PI controllers to regulate the output DC-link voltage. The MCC controls the arm AC active power based on the steady state model of the DC-DC MMC while the PCC controls the arm AC active power based on a perturb and observe algorithm. Performance and effectiveness of the proposed control strategies are evaluated based on simulation studies under various operating conditions in the PSCAD/EMTDC software environment.

CHAPTER I

CONTROL OF THE DC-AC MMC FOR VARIABLE-SPEED DRIVE SYSTEMS

1.1 Glossary of terms

Number of inserted SMs in the upper arm of MMC phase-j	$n_{p,j}$
Number of inserted SMs in the lower arm of MMC phase-j	$n_{n,j}$
PWM reference waveform for the upper arm of MMC phase-j	$m_{p,j}$
PWM reference waveform for the lower arm of MMC phase-j	$m_{n,j}$
PWM reference waveform to control the circulating current in phase-leg j of the MMC	$m_{\text{circ},j}$
Fundamental frequency component of PWM reference waveform for ac-side phase-j voltage	m_j
Magnitude of m_j	m
Common-mode frequency component of PWM reference waveform for ac-side phase-j voltage	m_{cm}
Magnitude of m_{cm}	M_{cm}
Angular frequency of m_{cm}	ω_{cm}
Frequency of m_{cm}	f_{cm}
Phase-j upper-arm current in MMC	$i_{p,j}$
Phase-j lower-arm current in MMC	$i_{n,j}$
Circulating current in phase-j leg of MMC	$i_{\text{circ},j}$
MMC dc-link current	i_{dc}
Ac-side current in phase-j	i_j
Magnitude of ac-side current	I_o
Frequency of ac-side current	f_r
Ac-side power factor angle	ϕ
Fundamental frequency component of ac-side phase-j voltage	v_j
Common-mode frequency component of ac-side phase-j voltage	v_{cm}
Ac-load resistance	R_{load}
Ac-load inductance	L_{load}
Machine phase-j back-emf	e_j
Rotor flux magnitude	λ_m^r
Rotor speed	ω_r
Rotor angle	θ_r
Power losses of the MMC	P_{loss}

Low-frequency components in x	$\tilde{x}$
Three-phase vector of phase current/voltage x_j	$\mathbf{x}_{\text{abc}}$
Park's transformation matrix	T
Settling time of closed-loop qd current control system of the motor	$t_{s,\text{out}}$
Damping constant of closed-loop qd current control system of the motor	δ_{out}
Settling time of closed-loop circulating current control system	$t_{s,\text{int}}$
Time constant of closed-loop circulating current control system	T_{con}
Settling time of current filter	$t_{s,\text{filter}}$
Proportional controller gain of the motor qd current controller	K_p
Integral controller gain of the motor qd current controller	K_i
Proportional controller gain of the circulating current controller	K_{p1}

1.2 Introduction

The modular multilevel converter (MMC) has become one of the most attractive converter topologies for medium- and high-voltage/power applications due to its modularity and scalability. The MMC has been widely investigated for high-voltage direct current transmission systems [1–10], and is increasingly being investigated for medium-voltage adjustable-speed drive systems [11–21]. One of the main technical challenges associated with the operation of MMC under constant-torque low-speed operation of the MMC-based adjustable-speed drive system is the large magnitude of the submodule (SM) capacitor voltage ripple due to the inverse dependence of the SM capacitor voltage ripple on the speed of the machine. This leads to increased rating values of the converter and/or instability.

In the technical literature, a few control strategies have been proposed to reduce the SM capacitor voltage ripple of the MMC-based adjustable-speed drive systems under constant-torque low-speed operation [15–17, 19, 21]. The control strategies proposed in [15–17, 19, 21] are mainly based on using two additional degrees of freedom, i.e., a common-mode voltage at the ac-side and a circulating current within the phase-legs, to attenuate the low-frequency components of the SM capacitor voltage. Mitigation of the low-frequency components in the SM capacitor voltage results in the reduction of the peak-to-peak ripple of the SM capacitor voltage. The control strategy based on using sinusoidal common-mode voltage and circulating current to attenuate the low-frequency components of the SM capacitor voltage was, first, proposed in [15]. In [17], the sinusoidal common-mode voltage and circulating current are optimized in the intermediate-speed region to limit the SM capacitor voltage ripple and the peak value of the arm current. In [21], the SM capacitor voltage ripple is analysed with respect to the peak value of the sinusoidal common-mode voltage. In [19], control of an MMC-based adjustable-speed drive system over the complete operating speed region is proposed. The control strategy in [19] in the low-speed region is based on a sinusoidal common-mode voltage and circulating current. A control strategy in the low-speed region, based on using square-wave common-mode voltage and circulating current to attenuate the low-frequency components in the SM capacitor voltage and to reduce the peak value of the circulating current, is proposed in [16]. In [20], the control strategy in the intermediate-speed region based on optimizing the dc value of the SM capacitor voltage, is explored. However, the control strategies proposed in [15–17, 19, 21]

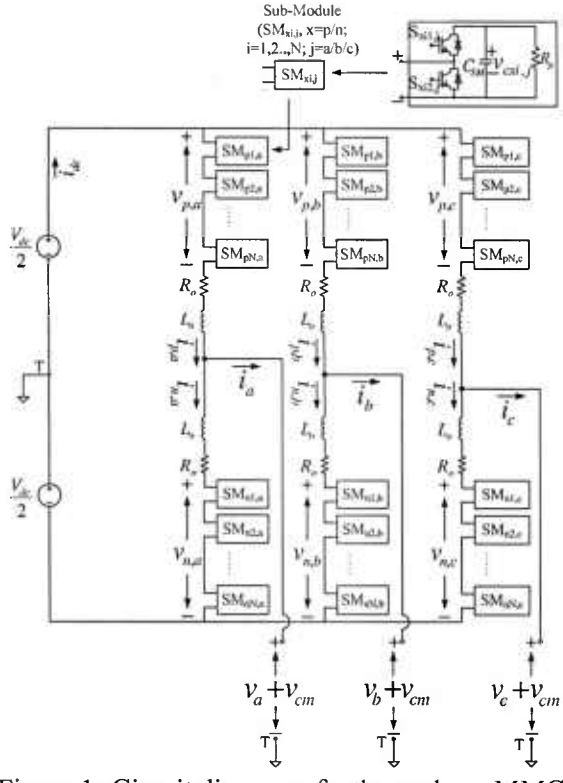

Figure 1: Circuit diagram of a three-phase MMC.

to reduce the SM capacitor voltage ripple in the low-speed region, have their own drawbacks. The control strategy proposed in [15, 17, 19, 21] requires a large circulating current, which increases the power losses and size of the components of the converter. The control strategy proposed in [16] is based on a square-wave circulating current. A square-wave circulating current requires a very large voltage across the arm inductor at its discontinuous points, which is practically difficult to attain and may cause control issues.

Stability analysis of the control strategies proposed/investigated for grid-connected MMCs has been explored in [22–24]. However, the stability analysis in [22] is only performed on specific states of the MMC with some assumptions on the stability of the other states of the system. The stability analysis in [24] is also performed on specific states of the MMC system. Moreover, the stability analysis in [23, 24] use the LaSalle's theorem on non-autonomous systems while the LaSalle's theorem is only applicable to the autonomous systems.

This project presents two new control strategies to reduce the SM capacitor voltage ripple under constant-torque low-speed operation of an MMC-based adjustable-speed drive system. The proposed control strategies are based on injecting a square-wave common-mode voltage at the ac-side and a circulating current within the phase-legs. The frequency spectrum of the injected circulating current consists of components in the vicinity of either the common-mode frequency or the common-mode frequency and third harmonic of the

common-mode frequency. This report also provides a theoretical comparison of the proposed control strategies with the existing control strategies. The proposed control strategies provide a superior performance compared to the existing control strategies, in terms of the peak/rms value of the circulating current and the SM capacitor voltage ripple. This paper presents a controller design methodology to systematically determine the controller gains of the proposed control strategies. The controller gains are designed such that the closed-loop circulating current control system settles much faster than the ac-side motor current control system. This report also proves the stability of the proposed control strategies and their design methodology based on Lyapunov analysis of singularly perturbed non-linear non-autonomous systems [25]. The stability analysis is performed on the complete MMC system. A set of experimental results for various case studies on a laboratory-scale prototype are provided to support the theoretical proof of stability of the proposed control strategies and their design methodology, and to confirm the superior performance of the proposed strategies over the existing strategy.

1.3 The MMC

The circuit diagram of a three-phase MMC is shown in Fig. 1. The structure of MMC is explained in [4]. The only addition to the structure explain in [4] is the resistor R_p, which represents the resistance used in the voltage sensing circuit of each SM capacitor.

1.3.1 Dynamic Model

As an extension of the work in [23], the capacitor voltage dynamics of the MMC can be summarized by

$$C_{\mathrm{SM}}\frac{dv_{cp,j}}{dt} = m_{p,j}\left(\frac{i_j}{2} + i_{\mathrm{circ},j} + \frac{i_{\mathrm{dc}}}{3}\right) - \frac{v_{cp,j}}{R_p}, \tag{1a}$$

$$C_{\mathrm{SM}}\frac{dv_{cn,j}}{dt} = m_{n,j}\left(-\frac{i_j}{2} + i_{\mathrm{circ},j} + \frac{i_{\mathrm{dc}}}{3}\right) - \frac{v_{cn,j}}{R_p}, \tag{1b}$$

where the PWM reference waveforms used to control the upper and lower arms of phase-leg j are given by

$$m_{p,j} = \frac{\left(1 - 2m_{\mathrm{circ},j}\right)}{2} - \frac{\left(m_j + m_{\mathrm{cm}}\right)}{2}, \tag{2a}$$

$$m_{n,j} = \frac{\left(1 - 2m_{\mathrm{circ},j}\right)}{2} + \frac{\left(m_j + m_{\mathrm{cm}}\right)}{2}. \tag{2b}$$

Moreover, the overall dynamics of the MMC can be summarized by

$$L_{\mathrm{eq}}\frac{di_j}{dt} = \frac{N}{2}\left(\frac{\left(m_j + m_{\mathrm{cm}}\right)}{2}v_{c,j}^{\Sigma} - \frac{\left(1 - 2m_{\mathrm{circ},j}\right)}{2}v_{c,j}^{\Delta}\right) - R_{\mathrm{eq}}i_j - \left(e_j + \tilde{v}_{\mathrm{cm}}\right), \tag{3a}$$

$$L_o\frac{di_{\text{circ},j}}{dt} = \frac{N}{2}\left(\frac{\left(m_j + m_{\text{cm}}\right)}{2}v_{c,j}^{\Delta} - \frac{\left(1 - 2m_{\text{circ},j}\right)}{2}v_{c,j}^{\Sigma}\right) + \frac{V_{\text{dc}}}{2} - \frac{R_o i_{\text{dc}}}{3} - R_o i_{\text{circ},j}, \tag{3b}$$

$$C_{\text{SM}}\frac{dv_{c,j}^{\Sigma}}{dt} = -\frac{\left(m_j + m_{\text{cm}}\right)}{2}i_j + \frac{2\left(1 - 2m_{\text{circ},j}\right)}{2}i_{\text{circ},j} - \frac{1}{R_p}v_{c,j}^{\Sigma} + \frac{2}{3}\frac{\left(1 - 2m_{\text{circ},j}\right)}{2}i_{\text{dc}}, \tag{3c}$$

$$C_{\text{SM}}\frac{dv_{c,j}^{\Delta}}{dt} = \frac{\left(1 - 2m_{\text{circ},j}\right)}{2}i_j - \frac{2\left(m_j + m_{\text{cm}}\right)}{2}i_{\text{circ},j} - \frac{1}{R_p}v_{c,j}^{\Delta} - \frac{2}{3}\frac{\left(m_j + m_{\text{cm}}\right)}{2}i_{\text{dc}}, \tag{3d}$$

where

$$v_{c,j}^{\Sigma} = \left(v_{cp,j} + v_{cn,j}\right), \tag{4a}$$

$$v_{c,j}^{\Delta} = \left(v_{cp,j} - v_{cn,j}\right), \tag{4b}$$

$$R_{\text{eq}} = R_{\text{load}} + \frac{R_o}{2}, \tag{4c}$$

$$L_{\text{eq}} = L_{\text{load}} + \frac{L_o}{2}. \tag{4d}$$

1.4 Low-Frequency Operation

Without adopting any specific control strategy, the peak-to-peak ripple of the SM capacitor voltages is given by [26]

$$\delta v_{c,\text{pp}} = \frac{I_o}{2C_{\text{SM}}\omega_r}\left(1 - \left(\frac{m\cos\phi}{2}\right)^2\right)^{\frac{3}{2}}. \tag{5}$$

As shown in (5), the peak-to-peak ripple of the SM capacitor voltages has an inverse dependency on the ac-side frequency and a direct dependency on the ac-side phase current magnitude. Consequently, under low-speed and startup conditions of constant-torque MMC-based adjustable-speed drive systems, the peak-to-peak ripple of the SM capacitor voltages becomes pronounced.

1.4.1 The Existing Sine-wave Strategy

The sine-wave control strategy to reduce the SM capacitor voltage ripple, hereafter referred to as the sine-wave strategy, is based on injecting a sinusoidal common-mode voltage and circulating current [15, 17, 19, 21]. The corresponding common-mode frequency

$$\frac{dv_{cp,j}}{dt} \approx -\frac{i_j}{C_{SM}}\left[\frac{\left(1-m_j^2\right)}{2}\left(\left(\frac{k_1}{3}-\frac{k_3}{2}\right)\cos(2\omega_{cm}t)+\left(\frac{k_1}{6}+\frac{k_3}{2}\right)\cos(4\omega_{cm}t)\right)+\frac{\left(1-m_j^2\right)}{2}\frac{k_3}{6}\cos(6\omega_{cm}t)\right.$$
$$-M_{cm}\left(1+m_j\right)\sum_{k=0}^{\infty}\frac{\sin\left((2k+1)\,\omega_{cm}t\right)}{\pi\,(2k+1)}+\left(1-m_j\right)\frac{\pi\left(1-m_j^2\right)}{8M_{cm}}\left(k_1\sin(\omega_{cm}t)+k_3\sin(3\omega_{cm}t)\right)$$
$$\left.-\frac{\left(1-m_j^2\right)}{2}\left(k_1\sin(\omega_{cm}t)+k_3\sin(3\omega_{cm}t)\right)\sum_{k=2}^{\infty}\frac{\sin\left((2k+1)\,\omega_{cm}t\right)}{(2k+1)}+\frac{\left(1-m_j^2\right)}{4}\left(1-k_1-\frac{k_3}{3}\right)\right]. \tag{8}$$

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component of the PWM reference waveform and the circulating current are given by

$$m_{cm}=\frac{v_{cm}}{\frac{V_{dc}}{2}}=M_{cm}\sin\left(\omega_{cm}t\right), \tag{6a}$$

$$i_{circ,j}=i_j\left(\frac{1-m_j^2}{M_{cm}}\right)\sin\left(\omega_{cm}t\right)+\frac{m_j i_j}{2}-\frac{i_{dc}}{3}. \tag{6b}$$

The PWM reference waveforms used to control the upper and lower arms of phase-leg j and to generate the common-mode voltage are given by (2a) and (2b). Substituting for m_{cm} from (6a), $m_{p,j}$ from (2a), and $i_{circ,j}$ from (6b) in (1a), the upper-arm phase-j SM capacitor voltages are deduced as

$$\frac{dv_{cp,j}}{dt}=\frac{\left(\frac{i_{dc}}{3}+i_{circ,j}+\frac{i_j}{2}\right)}{C_{SM}}\left(\frac{1-m_j-m_{cm}}{2}-m_{circ,j}\right)$$
$$\approx\frac{i_j}{C_{SM}}\left[\left(-\frac{m_jM_{cm}}{4}-\frac{M_{cm}}{4}\right.\right.$$
$$\left.+\frac{\left(1-m_j-m_j^2+m_j^3\right)}{2M_{cm}}\right)\sin\left(\omega_{cm}t\right)$$
$$\left.+\frac{\left(1-m_j^2\right)}{4}\cos(2\omega_{cm}t)\right]. \tag{7}$$

While deriving (7), a sufficiently fast closed-loop circulating current controller is assumed, which results in $i_{circ,j}=i_{circ,j,ref}$. Additionally, $m_{circ,j}$ and $\frac{1}{R_pC_{SM}}v_{cp,j}$ are considered negligible in (7). Considering appropriate phase shifts, similar expressions can be concluded for capacitor voltage ripple of the SMs in the lower arm as well. As shown in (7), the frequency spectrum of the SM capacitor voltages has been shifted from f_r to f_{cm} and since $f_{cm}\gg f_r$, the magnitude of the voltage ripple is reduced.

1.4.2 The Proposed Strategies

The proposed control strategies to reduce the SM capacitor voltage ripple, hereafter referred to as the proposed strategies, are based on injecting a square-wave common-mode voltage whose PWM reference waveform is expressed by

$$m_{\text{cm}} = \begin{cases} M_{\text{cm}} & \text{if } 0 < t \le \dfrac{1}{2f_{\text{cm}}} \\ -M_{\text{cm}} & \text{if } \dfrac{1}{2f_{\text{cm}}} < t \le \dfrac{1}{f_{\text{cm}}} \end{cases}. \tag{9}$$

The circulating current is derived based on cancellation of low-frequency components in the capacitor voltage ripple. The square-wave common-mode reference waveform in (9) can be expressed by its Fourier series expansion as

$$m_{\text{cm}} = \sum_{k=0}^{\infty} \frac{4M_{\text{cm}}}{\pi(2k+1)} \sin\left((2k+1)\omega_{\text{cm}} t\right). \tag{10}$$

The distinction between the two proposed strategies lies in the circulating current used to attenuate the low-frequency components of the capacitor voltage ripple of each SM. The circulating currents used in the two proposed strategies are:

Strategy I: A sinusoidal circulating current, with components in the vicinity of the common-mode frequency, as given by

$$i_{\text{circ},j} = i_j \left(\frac{1 - m_j^2}{\frac{4}{\pi} M_{\text{cm}}} \right) \sin(\omega_{\text{cm}} t) + \frac{m_j i_j}{2} - \frac{i_{\text{dc}}}{3}. \tag{11}$$

Substituting for m_{cm} from (10), $m_{p,j}$ from (2a), and $i_{\text{circ},j}$ from (11) in (1a) result in

$$\begin{aligned} \frac{dv_{cp,j}}{dt} \approx \frac{i_j}{C_{\text{SM}}} \Bigg[& \frac{\pi}{8M_{\text{cm}}} \left(1 - m_j\right)\left(1 - m_j^2\right) \sin(\omega_{\text{cm}} t) \\ & + \frac{1}{4}\left(1 - m_j^2\right) \cos(2\omega_{\text{cm}} t) \\ & - \frac{\left(1 - m_j^2\right) \sin(\omega_{\text{cm}} t)}{2} \sum_{k=1}^{\infty} \frac{\sin((2k+1)\omega_{\text{cm}} t)}{2k+1} \\ & - \frac{M_{\text{cm}}}{\pi}\left(1 + m_j\right) \sum_{k=0}^{\infty} \frac{\sin((2k+1)\omega_{\text{cm}} t)}{(2k+1)} \Bigg]. \end{aligned} \tag{12}$$

As shown by (12), the frequency spectrum of the SM capacitor voltage ripple is shifted to the vicinity of f_{cm}.

Strategy II: A sinusoidal circulating current, with components in the vicinity of the common-mode frequency and a third harmonic of the common-mode frequency, as

Table 1: Comparison of the two proposed strategies with the sine-wave strategy

Strategy	$m_{\text{cm,max}}$	$i_{\text{circ},j,\text{peak}}$	$I^2_{\text{circ},j,\text{rms}}$
Strategy I	$\frac{(1-m)}{2}\left(1+\sqrt{1-0.5\pi x}\right)$	$2I_{\text{cm1,NM1}}$ where $I_{\text{cm1,NM1}} = \frac{\pi I_o}{4(1-m)\left(1+\sqrt{1-0.5\pi x}\right)}$	$I^2_{\text{cm1,NM1}}$
Strategy II	$\frac{(1-m)}{2}\left(1+\sqrt{1-0.9\pi x}\right)$	$1.874I_{\text{cm1,NM2}}$ where $I_{\text{cm1,NM2}} = \frac{0.9\pi I_o}{4(1-m)\left(1+\sqrt{1-0.9\pi x}\right)}$	$\frac{10}{9}I^2_{\text{cm1,NM2}}$
Sine-Wave Strategy in [15]	$\frac{(1-m)}{2}\left(1+\sqrt{1-2x}\right)$	$2I_{\text{cm1,sine}}$ where $I_{\text{cm1,sine}} = \frac{I_o}{(1-m)\left(1+\sqrt{1-2x}\right)}$	$I^2_{\text{cm1,sine}}$

given by

$$i_{\text{circ},j} = i_j\left(\frac{1-m_j^2}{\frac{4}{\pi}M_{\text{cm}}}\right)(k_1\sin(\omega_{\text{cm}}t) + k_3\sin(3\omega_{\text{cm}}t)) + \frac{m_j i_j}{2} - \frac{i_{\text{dc}}}{3}. \tag{13}$$

k_1 and k_3 in (13) are determined to minimize the rms value of $i_{\text{circ},j}$ and to attenuate the low-frequency components of the SM capacitor voltage ripple.

Substituting for m_{cm} from (10), $m_{p,j}$ from (2a), and $i_{\text{circ},j}$ from (13) in (1a) results in (8). To mitigate the low-frequency components of the SM capacitor voltage ripple, the last term in (8) should be enforced to zero, i.e.,

$$1 - k_1 - \frac{k_3}{3} = 0. \tag{14}$$

Furthermore, as shown by (13), to minimize the rms value of the circulating currents, $k_1^2 + k_3^2$ needs to be minimized. Therefore, the coefficients k_1 and k_3 are determined by

$$\begin{aligned} &\text{Minimize } k_1^2 + k_3^2 \\ &\text{subject to } k_1 + \frac{k_3}{3} = 1 \end{aligned} \tag{15}$$

Solving (15) gives $k_1 = 0.9$ and $k_3 = 0.3$, which results in shifting the frequency spectrum of the SM capacitor voltage ripple to vicinity of f_{cm}, under low-frequency operation.

1.4.3 Comparison of the Proposed Strategies with the Sine-Wave Strategy

As discussed in Section 1.2, the control strategy based on injecting a square-wave common-mode voltage and circulating current [16], may raise control issues. Therefore, the performance of the proposed strategies are compared against the sine-wave strategy. Assuming the same peak value for the common-mode voltage reference used in the two proposed strategies and the sine-wave strategy in (6b), (11) and (13), the peak value of the

circulating current in the proposed strategies is reduced by 21.5% and 33.8%, respectively, when compared with the sine-wave strategy. The squared rms value of the circulating current, which is proportional to the additional conduction losses of the converter caused due to the presence of circulating currents, is also reduced by 38% and 44.2%, respectively. However, as compared to Strategy I, Strategy II requires a higher $m_{\text{circ},j}$, which, subsequently, limits the peak value of the common-mode voltage reference $m_{\text{cm,max}}$. To determine the peak value of the common-mode voltage reference signal for each of the proposed strategies, the following condition that represents the range of the upper-arm phase-j reference signal, $m_{p,j}$, should be satisfied:

$$\begin{aligned} & 0 \leq m_{p,j} \leq 1 \\ \Longrightarrow & 0 \leq \frac{1 - m_j - m_{\text{cm}}}{2} - m_{\text{circ},j} \leq 1. \end{aligned} \tag{16}$$

Based on (16), the limits of common-mode voltage reference signal for the two proposed strategies and the sine-wave strategy are listed in Table 1. The corresponding peak and the squared rms values of the circulating current for the three strategies are also provided in Table 1. The variable x in Table 1 is defined as

$$x = \frac{4 I_o L_o \omega_{\text{cm}}}{V_{\text{dc}} (1 - m)^2}. \tag{17}$$

Equation 16 along with the limits determined in Table 1 for the common-mode voltage reference signal, help prevent over-modulation.

1.5 Controller Design Methodology

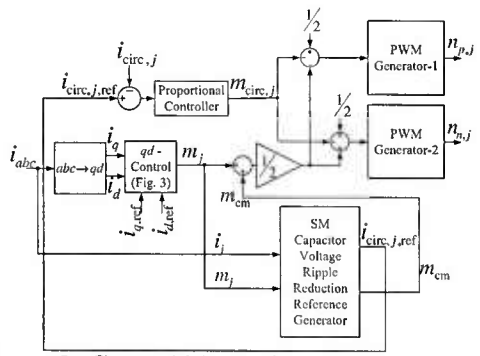


Figure 2: Control block diagram of the MMC.

A summary of the MMC control in MMC-based adjustable-speed PMSM drive systems with either of the proposed strategies or the sine-wave strategy is provided in Figs. 2-3. The control of MMC comprises the motor qd current control along with the circulating current control. The corresponding closed-loop systems are shown in Figs. 4-5.

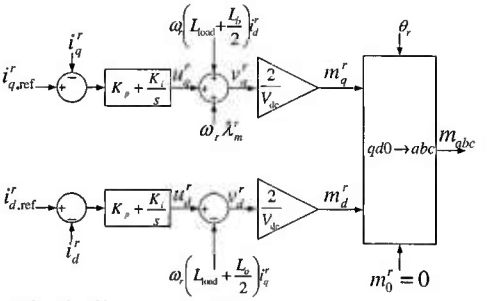


Figure 3: Block diagram of the motor qd current controller.

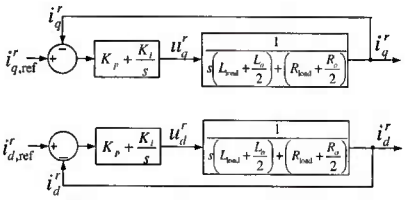


Figure 4: Block diagram of the closed-loop motor qd current control system.

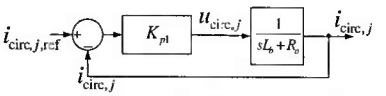


Figure 5: Block diagram of the closed-loop circulating current control system.

The PI controller parameters of the motor qd current controller are given by

$$K_p = 8\left(\frac{L_{\mathrm{eq}}}{t_{s,\mathrm{out}}}\right) - R_{\mathrm{eq}}, \tag{18a}$$

$$K_i = \frac{\left(R_{\mathrm{eq}} + K_p\right)^2}{4\delta^2_{\mathrm{out}} L_{\mathrm{eq}}}. \tag{18b}$$

The aforementioned PI controller parameters are designed on the basis of the closed-loop system in Fig. 4.

The settling time and time constant of the closed-loop circulating current control system shown in Fig. 5 are given by

$$t_{s,\mathrm{int}} = \frac{5L_o}{R_o + K_{pl}}, \tag{19a}$$

$$T_{\mathrm{con}} = \frac{L_o}{R_o + K_{pl}}. \tag{19b}$$

Based on the condition that the closed-loop circulating control system settles much faster than the closed-loop motor qd current control system and much slower than the current filter, the maximum and minimum settling times are defined as

$$t_{s,\mathrm{int,max}} = \frac{t_{s,\mathrm{out}}}{5}, \tag{20a}$$

$$t_{s,\mathrm{int,min}} = 5t_{s,\mathrm{filter}}. \tag{20b}$$

The corresponding proportional controller gains, based on (20) and (19a), are given by

$$K_{p1,\min_1} = 5\frac{L_o}{\frac{t_{s,\text{out}}}{5}} - R_o, \tag{21a}$$

$$K_{p1,\max} = 5\frac{L_o}{5t_{s,\text{filter}}} - R_o. \tag{21b}$$

To prevent the attenuation of the common-mode frequency components in the circulating currents, the maximum time constant of the closed-loop circulating current control system is defined as

$$T_{\text{con,max}} = \frac{1}{10 \times 2\pi f_{\text{cm}}}. \tag{22}$$

The corresponding proportional controller gain, based on (22) and (19b), is

$$K_{p1,\min_2} = 10 \times 2\pi f_{\text{cm}} L_o - R_o. \tag{23}$$

The constraints on K_{p1} are given by

$$\max\{K_{p1,\min_1}, K_{p1,\min_2}\} < K_{p1} < K_{p1,\max} \tag{24}$$

The controller gains of the motor qd current and circulating current control systems are designed using (18) and (24), respectively.

1.6 Closed-loop System

The closed-loop dynamics of the system, comprising the MMC-based adjustable-speed drive with the control strategy described in Sections 1.4 and 1.5, is provided in this section. The stability of this closed-loop system is proven in this section as well.

1.6.1 Closed-loop System Dynamics

From the motor qd current controller block diagram in Fig. 3, the fundamental frequency component of the PWM reference waveforms of the ac-side phase voltages are given by

$$\begin{aligned}\mathbf{m}_{abc} &= T(\theta_r)^{-1}\mathbf{m}^r_{qd0} \\ &= \frac{2K_p}{V_{\text{dc}}}(\mathbf{i}_{abc,\text{ref}} - \mathbf{i}_{abc}) \\ &\quad + \frac{2K_i}{V_{\text{dc}}}T^{-1}\int T(\mathbf{i}_{abc,\text{ref}} - \mathbf{i}_{abc})\,dt \\ &\quad + \frac{2\omega_r L_{\text{eq}}}{\sqrt{3}V_{\text{dc}}}X\mathbf{i}_{abc} + \frac{2}{V_{\text{dc}}}\mathbf{e}_{abc},\end{aligned} \tag{25a}$$

$$X = \begin{pmatrix} 0 & -1 & 1 \\ 1 & 0 & -1 \\ -1 & 1 & 0 \end{pmatrix}. \tag{25b}$$

Based on the circulating current controller, the modulation indices in the *abc* domain to control the circulating currents, are given by

$$\begin{aligned}\mathbf{m}_{\text{circ},abc} &= \begin{pmatrix} m_{\text{circ},a} & m_{\text{circ},b} & m_{\text{circ},c} \end{pmatrix}^{\text{T}} \\ &= \frac{K_{p1}}{V_{\text{dc}}} \left(\mathbf{i}_{\text{circ},abc,\text{ref}} - \mathbf{i}_{\text{circ},abc} \right). \end{aligned} \tag{26}$$

Expanding the dynamic model of MMC from (3) to all the phases, substituting for $\mathbf{m}_{abc}$ from (25) and $\mathbf{m}_{\text{circ},abc}$ from (26), linearizing the resulting system about its operating/reference point ($\mathbf{i}_{abc,\text{ref}}$, $\mathbf{i}_{\text{circ},abc,\text{ref}}$, $\mathbf{v}^{\Sigma}_{c,abc,\text{op}} = \frac{2V_{\text{dc}}}{N}\mathbf{1}$, $\mathbf{v}^{\Delta}_{c,abc,\text{op}} = \mathbf{0}$) by neglecting the higher-order terms in the Taylor series expansion, and removing the stationary ripples results in the following state-space equation

$$\frac{d\mathbf{x}}{dt} = A(t)\mathbf{x}(t) + \mathbf{d}(t, \mathbf{x}), \tag{27a}$$

$$A(t) = \begin{pmatrix} A_3 & 0 & A_4 & A_5 \\ 0 & A_6 & A_7 & A_8 \\ A_{10} & A_{11} & A_{12} & 0 \\ A_{14} & A_{15} & 0 & A_{16} \end{pmatrix}, \tag{27b}$$

$$\mathbf{d}(t, \mathbf{x}) = \begin{pmatrix} A_2^{\text{T}} & 0 & A_9^{\text{T}} & A_{13}^{\text{T}} \end{pmatrix}^{\text{T}} \int T\delta\mathbf{i}_{abc}dt, \tag{27c}$$

where

$$\delta\mathbf{i}_{abc} = \mathbf{i}_{abc} - \mathbf{i}_{abc,\text{ref}}, \tag{28a}$$

$$\delta\mathbf{i}_{\text{circ},abc} = \mathbf{i}_{\text{circ},abc} - \mathbf{i}_{\text{circ},abc,\text{ref}}, \tag{28b}$$

$$\delta\mathbf{v}^{\Sigma}_{c,abc} = \mathbf{v}^{\Sigma}_{c,abc} - \frac{2V_{\text{dc}}}{N}\mathbf{1}, \tag{28c}$$

$$\delta\mathbf{v}^{\Delta}_{c,abc} = \mathbf{v}^{\Delta}_{c,abc}, \tag{28d}$$

$$\mathbf{x} = \begin{pmatrix} \delta\mathbf{i}^{\text{T}}_{abc} & \delta\mathbf{i}^{\text{T}}_{\text{circ},abc} & \delta\mathbf{v}^{\Sigma\text{T}}_{c,abc} & \delta\mathbf{v}^{\Delta\text{T}}_{c,abc} \end{pmatrix}^{\text{T}}, \tag{28e}$$

$$A_2 = T^{-1}\frac{K_i}{L_{\text{eq}}}, \tag{28f}$$

$$A_3 = -\frac{\left(K_p + R_{\text{eq}}\right)}{L_{\text{eq}}} I_3 + \frac{\omega_r}{\sqrt{3}} X, \tag{28g}$$

$$\begin{aligned} A_4 = {} & \frac{N\omega_r}{2\sqrt{3}V_{\text{dc}}} \text{diag}\left(\left(X\mathbf{i}_{abc,\text{ref}} \right)^{\text{T}} \right) + \frac{Nm_{\text{cm}}}{4L_{\text{eq}}} I_3 \\ & + \frac{N}{2V_{\text{dc}}L_{\text{eq}}} \text{diag}\left(\mathbf{e}^{\text{T}}_{abc} \right), \end{aligned} \tag{28h}$$

$$A_5 = -\frac{N}{4L_{\text{eq}}} I_3, A_6 = -\frac{K_{p1} + R_o}{L_o} I_3, \tag{28i}$$

$$A_7 = -\frac{N}{4L_o} I_3, A_8 = A_4 \frac{L_{\text{eq}}}{L_o}, \tag{28j}$$

$$A_9 = \frac{K_i}{V_{\text{dc}} C_{\text{SM}}} \text{diag}\left(\mathbf{i}_{abc,\text{ref}}^{\text{T}}\right) T^{-1}, \tag{28k}$$

$$A_{10} = \frac{1}{V_{\text{dc}} C_{\text{SM}}} \left(\text{diag} K_p \left(\mathbf{i}_{abc,\text{ref}}^{\text{T}}\right) - \text{diag}\left(\mathbf{e}_{abc}^{\text{T}}\right)\right) - \frac{m_{\text{cm}}}{2C_{\text{SM}}} I_3$$
$$- \frac{\omega_r L_{\text{eq}}}{\sqrt{3} V_{\text{dc}} C_{\text{SM}}} \left(\text{diag}\left((X\mathbf{i}_{abc,\text{ref}})^{\text{T}}\right) + \text{diag}\left(\mathbf{i}_{abc,\text{ref}}^{\text{T}}\right) X\right), \tag{28l}$$

$$A_{11} = \frac{1}{C_{\text{SM}}} I_3 + \frac{2K_{p1}}{V_{\text{dc}} C_{\text{SM}}} \text{diag}\left(\mathbf{i}_{\text{circ},abc,\text{ref}}^{\text{T}}\right) + \frac{2K_{p1} i_{\text{dc}}}{3V_{\text{dc}} C_{\text{SM}}} I_3, \tag{28m}$$

$$A_{12} = A_{16} = -\frac{1}{R_p C_{\text{SM}}} I_3, \tag{28n}$$

$$A_{13} = \frac{2K_i}{V_{\text{dc}} C_{\text{SM}}} \text{diag}\left(\mathbf{i}_{\text{circ},abc,\text{ref}}^{\text{T}} + \frac{i_{\text{dc}}}{3} \mathbf{1}^{\text{T}}\right) T^{-1}, \tag{28o}$$

$$A_{14} = \frac{1}{2C_{\text{SM}}} I_3 + \frac{2K_p}{V_{\text{dc}} C_{\text{SM}}} \text{diag}\left(\mathbf{i}_{\text{circ},abc,\text{ref}}^{\text{T}} + \frac{i_{\text{dc}}}{3} \mathbf{1}^{\text{T}}\right)$$
$$- \frac{2\omega_r L_{\text{eq}}}{\sqrt{3} V_{\text{dc}} C_{\text{SM}}} \text{diag}\left(\mathbf{i}_{\text{circ},abc,\text{ref}}^{\text{T}} + \frac{i_{\text{dc}}}{3} \mathbf{1}^{\text{T}}\right) X, \tag{28p}$$

$$A_{15} = \frac{K_{p1}}{V_{\text{dc}} C_{\text{SM}}} \text{diag}\left(\mathbf{i}_{abc,\text{ref}}^{\text{T}}\right) - \frac{2}{V_{\text{dc}} C_{\text{SM}}} \text{diag}\left(\mathbf{e}_{abc}^{\text{T}}\right) - \frac{m_{\text{cm}}}{C_{\text{SM}}} I_3$$
$$- \frac{2\omega_r L_{\text{eq}}}{\sqrt{3} V_{\text{dc}} C_{\text{SM}}} \text{diag}\left((X\mathbf{i}_{abc,\text{ref}})^{\text{T}}\right), \tag{28q}$$

$\odot$ represents the Hadamard product, and $\mathbf{1} = \begin{pmatrix} 1 & 1 & 1 \end{pmatrix}^{\text{T}}$. Equations (27) and (28) represent the linearized closed-loop dynamics of the MMC-based adjustable-speed drive system with the control strategy described in Section 1.5. The system described in (27) and (28) is a non-autonomous system and its stability, based on Lyapunov analysis of singularly perturbed non-linear non-autonomous systems [25], is proven in the next section.

1.6.2 Stability Analysis of the Closed-loop System

The system described by (27) and (28) is re-written as

$$\frac{d\mathbf{x}_1}{dt} = A_r(t)\mathbf{x}_1 + \mathbf{d}_1(t, \mathbf{x}_1, \mathbf{x}_2), \tag{29a}$$

$$\mu \frac{d\mathbf{x}_2}{dt} = A_b \mathbf{x}_2 + \mathbf{d}_2(t, \mathbf{x}_1, \mu), \tag{29b}$$

where

$$\mu = \frac{K_p}{R_p C_{\mathrm{SM}}} \frac{1}{K_{p1} + R_o}, \tag{30a}$$

$$\mathbf{x}_1 = \begin{pmatrix} \delta \mathbf{i}_{abc}^{\mathrm{T}} & \delta \mathbf{v}_{c,abc}^{\Sigma\,\mathrm{T}} & \delta \mathbf{v}_{c,abc}^{\Delta\,\mathrm{T}} \end{pmatrix}^{\mathrm{T}}, \tag{30b}$$

$$\mathbf{x}_2 = \delta \mathbf{i}_{\mathrm{circ},abc}, \tag{30c}$$

$$A_b = -\frac{K_p}{R_p C_{\mathrm{SM}} L_o}, \tag{30d}$$

$$A_r(t) = \begin{pmatrix} A_3 & A_4 & A_5 \\ A_{10} & A_{12} & 0 \\ A_{14} & 0 & A_{16} \end{pmatrix}, \tag{30e}$$

$$\mathbf{d}_2(t, \mathbf{x}_1, \mu) = \begin{pmatrix} 0 & \mu A_7 & \mu A_8 \end{pmatrix} \mathbf{x}_1, \tag{30f}$$

$$\mathbf{d}_1(t, \mathbf{x}_1, \mathbf{x}_2) = \begin{pmatrix} 0 & A_{11}^{\mathrm{T}} & A_{15}^{\mathrm{T}} \end{pmatrix}^{\mathrm{T}} \mathbf{x}_2 + \begin{pmatrix} A_2^{\mathrm{T}} & A_9^{\mathrm{T}} & A_{13}^{\mathrm{T}} \end{pmatrix}^{\mathrm{T}} \int T \delta \mathbf{i}_{abc} dt. \tag{30g}$$

Based on (18a), (21a), and (24), $\frac{K_{p1} + R_o}{K_p}$ is large. Additionally, $R_p C_{\mathrm{SM}}$ is very large due to the large resistor R_p typically used in the voltage sensing circuit. Consequently, based on (30a), $\mu \to 0$. That is, the system in (29) and (30) can be considered as a combination of a reduced-order system and a boundary-layer system as $\mu \to 0$.

Substituting $\mu = 0$ in (29b) results in

$$A_b \mathbf{x}_2 = 0 \Longrightarrow \mathbf{x}_2 = 0. \tag{31}$$

The solution of $\mathbf{x}_2$ in (29b) with $\mu = 0$ is given by (31). Substituting $\mathbf{x}_2$ from (31) in (29a) results in a reduced-order system for the system described by (29) and (30), which is given by

$$\frac{d\mathbf{x}_1}{dt} = A_r(t)\mathbf{x}_1 + \mathbf{d}_{1,n}(t, \mathbf{x}_1), \tag{32a}$$

$$\mathbf{d}_{1,n}(t, \mathbf{x}_1) = \begin{pmatrix} A_2^{\mathrm{T}} & A_9^{\mathrm{T}} & A_{13}^{\mathrm{T}} \end{pmatrix}^{\mathrm{T}} \int T \delta \mathbf{i}_{abc} dt \tag{32b}$$

A "fast time" $\tau = \frac{t}{\mu}$ and a boundary-layer state $\mathbf{x}_b(\tau) = \mathbf{x}_2(\mu\tau) = \mathbf{x}_2(t)$ are defined. Then, the boundary-layer system for the system described by (29) and (30) is given by

$$\begin{aligned} \frac{d\mathbf{x}_b}{d\tau} &= A_b \mathbf{x}_b + \mathbf{d}_2(t, \mathbf{x}_1, 0) \\ &= -\frac{K_p}{R_p C_{\mathrm{SM}} L_o} \mathbf{x}_b. \end{aligned} \tag{33}$$

The boundary-layer system given by (33) is exponentially stable, uniformly for any $(t,\mathbf{x}_1)$, with the eigen-value of $-\dfrac{K_p}{R_pC_{\mathrm{SM}}L_o}$ of algebraic multiplicity 3.

The reduced-order system described by (32) can be re-written as

$$\frac{d\mathbf{x}_{1,1}}{dt} = A_{r,r}\mathbf{x}_{1,1} + \mathbf{d}_{1,1}(t, \mathbf{x}_{1,2}), \tag{34a}$$

$$\mu_1\frac{d\mathbf{x}_{1,2}}{dt} = A_{r,b}(t,\mu_1)\mathbf{x}_{1,2} + \mathbf{d}_{1,2}(t, \mathbf{x}_{1,1}, \mathbf{x}_{1,2}, \mu_1), \tag{34b}$$

where

$$\mu_1 = \frac{1}{R_pC_{\mathrm{SM}}K_p}, \tag{35a}$$

$$\mathbf{x}_{1,1} = \left(\delta\mathbf{v}_{c,abc}^{\Sigma\,\mathrm{T}} \quad \delta\mathbf{v}_{c,abc}^{\Lambda\,\mathrm{T}}\right)^{\mathrm{T}}, \tag{35b}$$

$$\mathbf{x}_{1,2} = \delta\mathbf{i}_{abc}, \tag{35c}$$

$$A_{r,r} = \begin{pmatrix} -\dfrac{1}{R_pC_{\mathrm{SM}}}I_3 & 0 \\ 0 & -\dfrac{1}{R_pC_{\mathrm{SM}}}I_3 \end{pmatrix}, \tag{35d}$$

$$A_{r,b}(t,\mu_1) = -\frac{\left(\dfrac{1}{R_pC_{\mathrm{SM}}} + \mu_1 R_{\mathrm{eq}}\right)}{L_{\mathrm{eq}}}I_3 + \mu_1\frac{\omega_r}{\sqrt{3}}X, \tag{35e}$$

$$\begin{aligned}\mathbf{d}_{1,1}(t, \mathbf{x}_{1,2}) = {} & \left(A_{10}^{\mathrm{T}} \quad A_{14}^{\mathrm{T}}\right)^{\mathrm{T}}\mathbf{x}_{1,2} \\ & + \left(A_9^{\mathrm{T}} \quad A_{13}^{\mathrm{T}}\right)^{\mathrm{T}}\int T\mathbf{x}_{1,2}dt,\end{aligned} \tag{35f}$$

$$\begin{aligned}\mathbf{d}_{1,2}(t, \mathbf{x}_{1,1}, \mathbf{x}_{1,2}, \mu_1) = {} & \left(\mu_1A_4 \quad \mu_1A_5\right)\mathbf{x}_{1,1} \\ & + \mu_1A_2\int T\mathbf{x}_{1,2}dt.\end{aligned} \tag{35g}$$

Since $K_pR_pC_{\mathrm{SM}}$ is large due to the large R_p as explained earlier, $\mu_1 \to 0$. As $\mu_1 \to 0$, the system described by (34) and (35) can be considered as a combination of a reduced-order system and a boundary-layer system.

Substituting $\mu_1 = 0$ in (34b) results in

$$A_{r,b}(t,0)\mathbf{x}_{1,2} = 0 \Longrightarrow \mathbf{x}_{1,2} = 0 \tag{36}$$

The solution of $\mathbf{x}_{1,2}$ in (34b) with $\mu_1 = 0$ is given by (36). Substituting $\mathbf{x}_{1,2}$ from (36) in (34a) results in the reduced-order system for the system described by (34) and (35) and is given by

$$\frac{d\mathbf{x}_{1,1}}{dt} = A_{r,r}\mathbf{x}_{1,1}. \tag{37}$$

The reduced-order system given by (37), (35b), and (35d), is exponentially stable with the eigen-value of $-\frac{1}{R_p C_{SM}}$ of algebraic multiplicity 6.

Furthermore, define another "fast time" $\tau_1 = \frac{t}{\mu_1}$ and let $\mathbf{x}_{1,b}(\tau_1) = \mathbf{x}_{1,2}(\mu_1 \tau_1) = \mathbf{x}_{1,2}(t)$. Then, the boundary-layer system for the system described by (34) and (35) is given by

$$\begin{aligned} \frac{d\mathbf{x}_{1,b}}{d\tau_1} &= A_{r,b}(t,0)\mathbf{x}_{1,b} + \mathbf{d}_{1,2}(t, \mathbf{x}_{1,1}, \mathbf{x}_{1,b}, 0) \\ &= -\frac{1}{R_p C_{SM} L_{eq}} \mathbf{x}_{1,b}. \end{aligned} \tag{38}$$

The system described by (38) is exponentially stable, uniformly for any $(t,\mathbf{x}_{1,1})$, with the eigen-value of $-\frac{1}{R_p C_{SM} L_{eq}}$ of algebraic multiplicity of 3.

Based on the aforementioned results, the following statements are true for the system described by (34) and (35):

1. The origin of the reduced-order system given by (37), (35b) and (35d) is exponentially stable.
2. The origin of the boundary-layer system given by (38) is exponentially stable, uniformly for any $(t,\mathbf{x}_{1,1})$.

Then, by Theorem 11.4 in [25] for singularly perturbed systems, the origin of the system described by (34) and (35) is exponentially stable, for small μ_1. That is, the origin of the reduced-order system for the system described by (29) and (30) is exponentially stable, for small μ_1.

Summarizing the results for the system described by (29) and (30), the following statements can be concluded:

1. The origin of the reduced-order system given by (34) and (35) is exponentially stable.
2. The origin of the boundary-layer system given by (33) is exponentially stable, uniformly for any $(t,\mathbf{x}_1)$.

Therefore, by Theorem 11.4 in [25] for singularly perturbed systems, the origin of the system described by (29) and (30) is exponentially stable, for small μ and μ_1. Consequently, the proof of stability of the closed-loop system comprising the MMC-based adjustable-speed drive with the control strategy described in Section 1.4 and 1.5, is concluded.

1.7 Experimental Results

The experimental results on a laboratory-scale MMC system for the following case studies are demonstrated in this section: (i) startup, (ii) step change in torque, and (ii) steady state. The aforementioned experimental case studies provide support to the theoretical proof of stability of the proposed control strategies and their design methodology, and verify the superior performance of the proposed strategies over the sine-wave strategy. The parameters of the PMSM load and the MMC system are listed in Tables 2 and 3, respectively.

Table 2: PMSM Parameters

Quantity	Value
Rated power	2 kVA
Rated voltage (line-to-line)	109 V
Rated electrical frequency f_r	120 Hz
R_{load}	0.22 Ω
L_{load}	6.03 mH
Number of poles pairs (P/2)	2

Table 3: MMC Parameters

Quantity	Value
Nominal power	10 kVA
L_o	2.2 mH
R_o	88.88 mΩ
Nominal net dc voltage V_{dc}	200 V
SM capacitance C_{SM}	1.41 mF
Number of SMs per arm N	4
IGBT voltage drop	1.5 V
IGBT resistance	22.2 mΩ
Diode voltage drop	1.25 V
Diode resistance	7 mΩ
Carrier frequency f_c	3.6 kHz
Sampling time $f_s = \frac{1}{T_s}$	18 kHz

1.7.1 Startup Operation

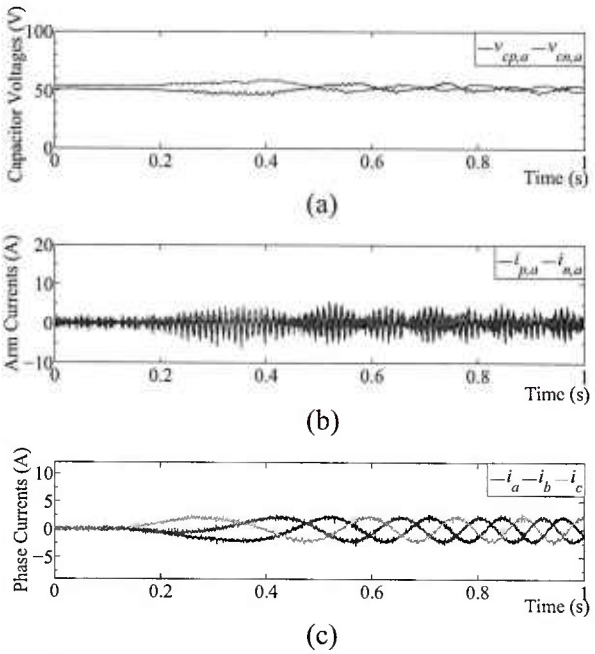


Figure 6: MMC experimental waveforms for Strategy I during startup: (a) phase-a SM capacitor voltages, (b) phase-a arm currents, and (c) ac-side currents.

The startup of the PMSM involves the acceleration of the PMSM from zero to 240 rpm with motor qd current references of $i_{q,\text{ref}} = 2.12$ A and $i_{d,\text{ref}} = 0$ A. The startup process is performed based on both of the proposed strategies with $f_{\text{cm}} = 90$ Hz.

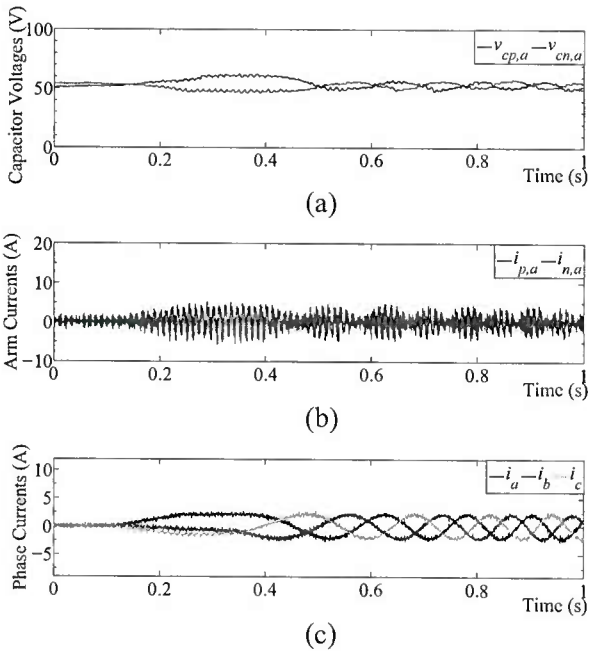


Figure 7: MMC experimental waveforms for Strategy II during startup: (a) phase-a SM capacitor voltages, (b) phase-a arm currents, and (c) ac-side currents.

The experimental results of the MMC system during the startup of PMSM using Strategies I and II are shown in Figs. 6 and 7, respectively. The startup of PMSM with Strategies I and II is initiated at t = 1.8 s and t = 2.4 s, respectively. The capacitor voltages of two SMs, one in the upper arm and one in the lower arm of phase-a, are shown in Figs. 6(a) and 7(a). As shown in Figs. 6(a) and 7(a), the peak-to-peak ripple of the SM capacitor voltages during the startup process using Strategies I and II is maintained within 10 V and 13 V, respectively. The phase-a arm currents during the startup process are shown in Figs. 6(b) and 7(b). In addition to the low-frequency ac-side motor current, a high-frequency circulating current is observed in the arm currents during the stratup process. The ac-side motor currents during the startup process are shown in Figs. 6(c) and 7(c).

1.7.2 Step Change in Torque

A step change in the torque reference is equivalent to a step change in $i_{q,\text{ref}}$ [27]. For a change in $i_{q,\text{ref}}$ from 2.82 A to 1.41 A and with $i_{d,\text{ref}}$ = 0 A, the experimental results of the MMC system operating with both of the proposed strategies and using f_{cm} = 90 Hz are shown and explained in this section.

The experimental results of the MMC system with a step change in the torque reference of the PMSM are shown in Figs. 8 and 9, respectively. At t = 2.4 s, the machine torque is stepped up from 1 Nm to 0.5 Nm. The capacitor voltage of two SMs, one in the upper arm and one in the lower arm of phase-a, subsequent to the step change in the torque are shown in Figs. 8(a) and 9(a). As shown in Figs. 8(a) and 9(a), subsequent to the transience associated with the step change in the torque, the peak-to-peak ripple of the SM capacitor voltages is well maintained. The phase-a arm currents during the step change in the torque

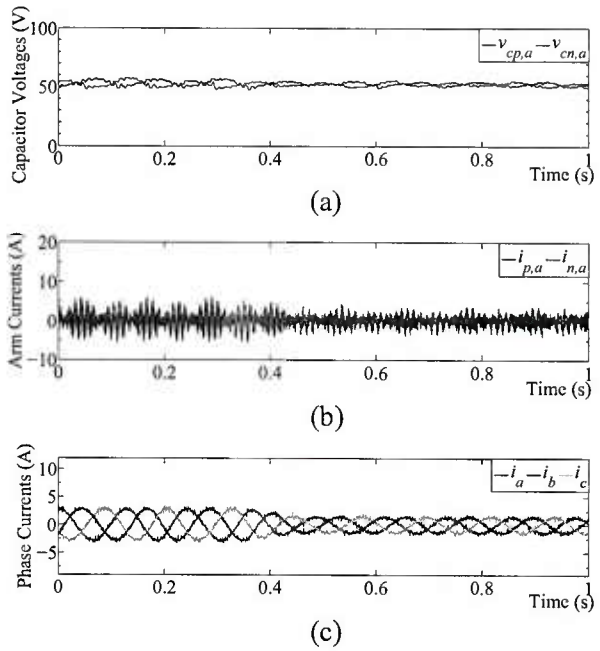


Figure 8: MMC experimental waveforms for Strategy I during step change in the torque: (a) phase-*a* SM capacitor voltages, (b) phase-*a* arm currents, and (c) ac-side currents.

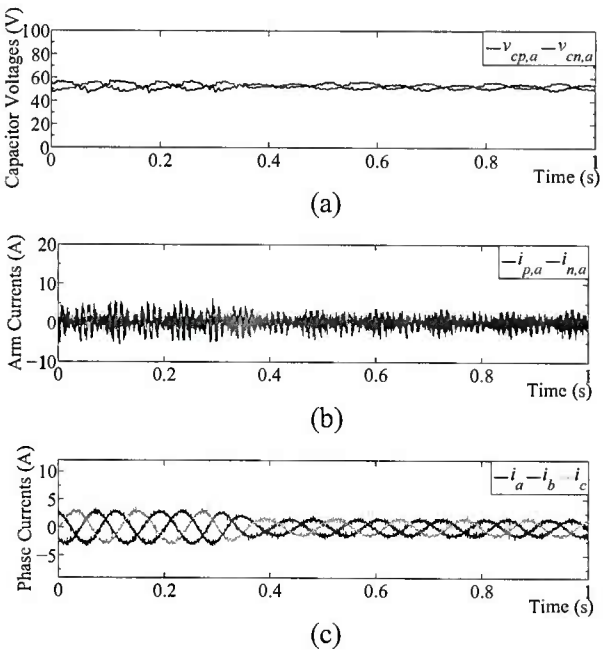


Figure 9: MMC experimental waveforms for Strategy II during step change in the torque: (a) phase-*a* SM capacitor voltages, (b) phase-*a* arm currents, and (c) ac-side currents.

are shown in Figs. 8(b) and 9(b). The ac-side motor currents subsequent to the step change in the torque are shown in Figs. 8(c) and 9(c).

1.7.3 Steady-state

The experimental results of the MMC system driving the PMSM at 240 rpm speed and with a peak ac-side current of I_o = 4.24 A using the sine-wave strategy, and the proposed Strategies I and II are shown in Figs. 10 to 12, respectively. The common-mode frequency used in all the strategies is f_{cm} = 30 Hz. The capacitor voltage of two SMs, one in the upper arm and one in the lower arm of phase-*a*, for the three strategies are shown in Figs. 10(a) to 12(a). As shown in Figs. 10(a) to 12(a), the peak-to-peak ripple of the SM capacitor voltages for the sine-wave strategy, and Strategies I and II is maintained within 22 V, 19 V, and 16 V, respectively. The phase-*a* arm currents are shown in Figs. 10(b) to 12(b). As shown in Figs. 10(b) to 12(b), the peak value of the arm current for the sine-wave strategy, and Strategies I and II are 10 A, 7.5 A, and 6 A, respectively. The ac-side currents for the three strategies are shown in Figs. 10(c) to 12(c). The experimental results highlight the superior performance of the proposed strategies over the sine-wave strategy, in terms of the peak-to-peak ripple of the SM capacitor voltage and the peak value of the arm current.

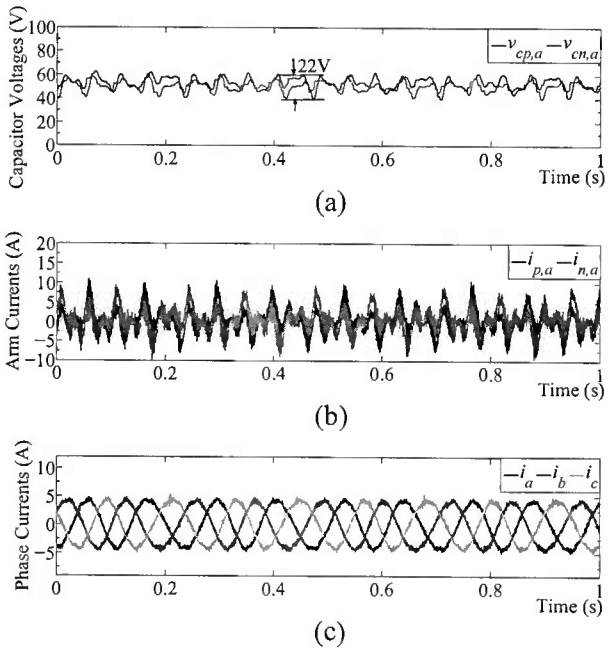


Figure 10: MMC experimental waveforms for the sine-wave strategy in steady-state: (a) phase-*a* SM capacitor voltages, (b) phase-*a* arm currents, and (c) ac-side currents.

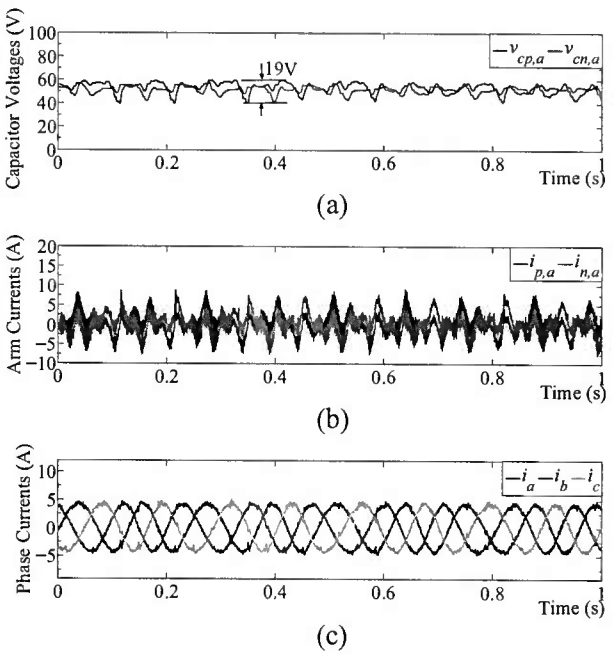


Figure 11: MMC experimental waveforms for Strategy I in steady-state: (a) phase-*a* SM capacitor voltages, (b) phase-*a* arm currents, and (c) ac-side currents.

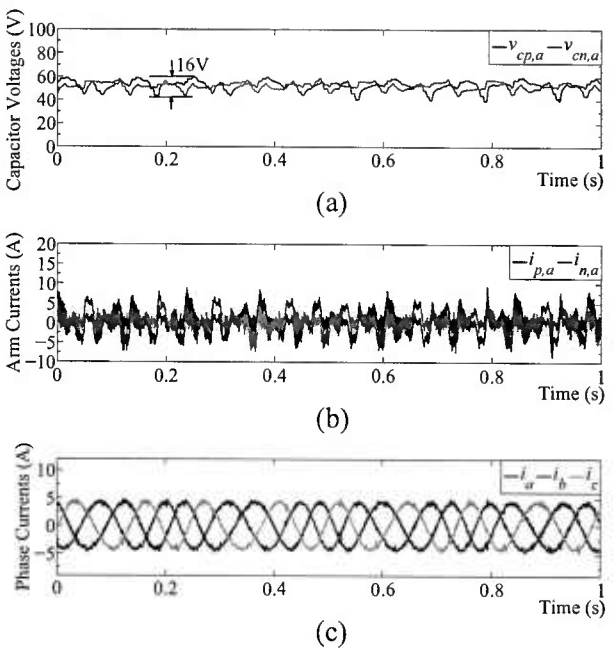


Figure 12: MMC experimental waveforms for Strategy II in steady-state: (a) phase-*a* SM capacitor voltages, (b) phase-*a* arm currents, and (c) ac-side currents.

CHAPTER II

CONTROL OF THE DC-DC MMC

2.1 Mathematical Modeling of the DC MMC

2.1.1 Basics of Operation

The circuit diagram of an M-phase-leg DC MMC is shown in Fig. 13 in which the DC-link 2 voltage v_{dc2} is greater than the DC-link 1 voltage v_{dc1}. The DC MMC consists of two arms per phase-leg, i.e., an upper arm (represented by superscript "p") and a lower arm (represented by superscript "n"). Each arm consists of series connection of N nominally identical half-bridge SMs and an arm inductor l. The output terminal/mid-point of each phase-leg is connected to the converter DC-link 1 terminal via a phase filtering inductor L.

Each SM of the DC MMC of Fig. 13 can provide two voltage levels at its terminal, i.e., zero or $v_C^{xi,j}$, $x \in \{p, n\}$; $i \in \{1, 2, ..., N\}$; $j \in \{1, 2, ..., M\}$, depending on the states of its complementary switches $S_{xi1,j}$ and $S_{xi2,j}$. Ideally, the average value of each SM capacitor voltage is maintained at v_{dc2}/N. The two switching states of SM-i in arm-x of phase-j are:

- $S_{xi1,j} = 1$ and $S_{xi2,j} = 0$: ON-state or inserted,
- $S_{xi1,j} = 0$ and $S_{xi2,j} = 1$: OFF-state or bypassed.

The number of phase-legs of the DC MMC should be chosen based on the power rating requirement. For high-power applications, multiple phase-legs are required to increase the power rating of the converter. For the case of $M = 1$, a series LC filter is inserted to establish a path for the AC circulating current [28]. For the case of $M > 1$, the phase-legs operate in an interleaved manner, i.e., the gating signals among phase-legs are identical with a phase shift of $\frac{2\pi}{M}$.

The voltage of each arm of the DC MMC, i.e., $v_{arm}^{x,j}$, $x \in \{p, n\}$; $j \in \{1, 2, ..., M\}$, is controlled by the number of inserted SMs. During normal operation, the voltage of each arm consists of a DC as well as an AC component. The lower arm DC voltage component is determined by v_{dc1} while the upper arm DC voltage component is determined by the ratio of v_{dc1}/v_{dc2}. The AC voltage component, on the other hand, is controlled to drive an AC circulating current component within each phase-leg, exchanging active AC power between the upper and lower arms of the corresponding phase-leg.

For proper operation of the converter, the following constraints must be satisfied: (i) the half-bridge SM can only insert a positive voltage in the ON-state, thus the instantaneous arm voltage must be greater than zero, and (ii) the maximum instantaneous arm voltage must be smaller than the DC-link 2 voltage. Therefore, the maximum amplitudes of the AC component of the upper and lower arm voltages are determined by:

$$|\tilde{v}_{arm,ac}^{p}|_{max} = \text{Min}[v_{arm,dc}^{p}, (v_{dc2} - v_{arm,dc}^{p})], \tag{39}$$

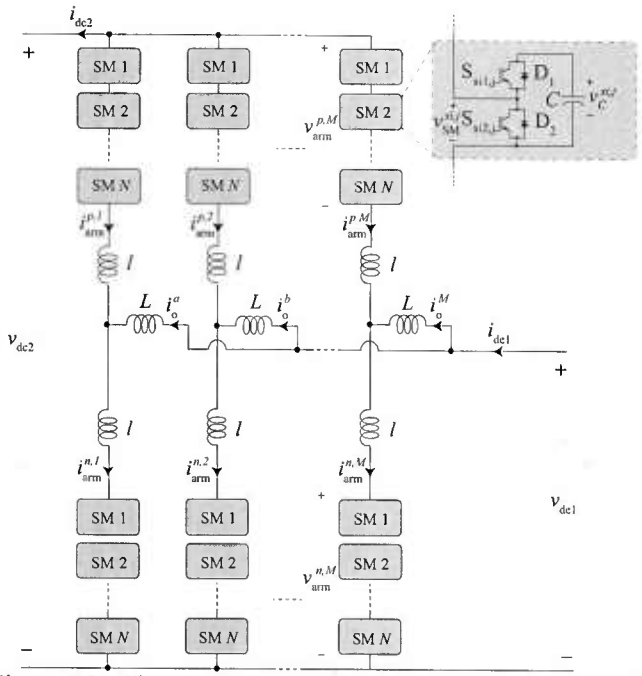


Figure 13: Circuit diagram of an M-phase-leg DC MMC.

$$|\tilde{v}^{n}_{\text{arm,ac}}|_{\max} = \text{Min}[v^{n}_{\text{arm,dc}}, (v_{\text{dc2}} - v^{n}_{\text{arm,dc}})]. \tag{40}$$

2.1.2 Phasor-domain Steady-state Model

To develop a mathematical model of the DC MMC, the following assumptions are made:

1. The number of SMs per arm is assumed to be considerably large. Based on this assumption, the arm voltages can be represented by ideal voltage sources;
2. The converter components are ideal and lossless, i.e., $P_{\text{in}} = P_{\text{out}}$;
3. A proper capacitor voltage balancing strategy is adopted to maintain the SM capacitor voltages balanced at their nominal values, i.e., v_{dc2}/N.

In deriving the steady state model of the converter, for the sake of simplicity, only one phase-leg is considered. Nevertheless, the mathematical model of one phase-leg can be extended to the case of an M-phase-leg DC MMC. Fig. 14 shows the corresponding equivalent circuit of a single phase-leg of the DC MMC, where $v^{x}_{\text{arm,dc}}$ and $\tilde{v}^{x}_{\text{arm,ac}}$ represent the DC and AC components of the arm voltage, respectively, $i^{x}_{\text{arm,dc}}$ and $\tilde{i}^{x}_{\text{arm,ac}}$ represent the DC and AC components of the arm current, respectively, $i_{o,\text{dc}}$ represents the DC component of the phase current, and $\tilde{i}_{o,\text{ac}}$ represents the AC component of the phase current, which should be ideally equal to zero. The cascaded SMs within each arm are represented by ideal controllable voltage sources. Since the converter consists of M identical phase-legs, the rated DC power is equally shared among the phase-legs.

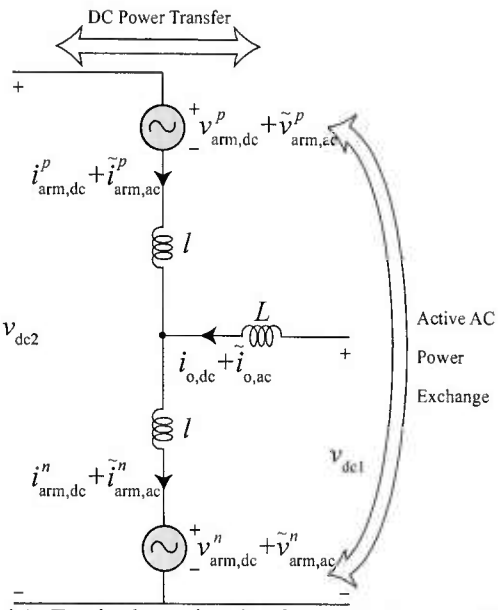


Figure 14: Equivalent circuit of one phase-leg of the DC MMC.

Based on the superposition principle, the converter phase-leg equivalent circuit can be decomposed into DC and AC sub-circuits. To derive the DC equations, a DC equivalent circuit of a single phase-leg is obtained and shown in Fig. 15. Based on the assumption of a lossless conversion, the DC components of the upper and lower arm voltages and currents can be represented by:

$$v^p_{arm,dc} = v_{dc2} - v_{dc1}, \tag{41}$$

$$v^n_{arm,dc} = v_{dc1}, \tag{42}$$

$$i^p_{arm,dc} = -\frac{i_{dc2}}{M}, \tag{43}$$

$$i^n_{arm,dc} = \frac{i_{dc2}}{M}\left(\frac{v_{dc2}}{v_{dc1}} - 1\right). \tag{44}$$

The upper and lower arm DC power can be represented by:

$$P^p_{arm,dc} = \left(\frac{v_{dc1}}{v_{dc2}} - 1\right)\frac{P}{M}, \tag{45a}$$

$$P^n_{arm,dc} = -P^p_{arm,dc}, \tag{45b}$$

where P is the output power and is considered positive when power flows from the DC-link 1 to DC-link 2.

Based on the superposition, the upper and lower arm AC equivalent circuits of one phase-leg are shown in Figs. 16(a) and (b), respectively. In the AC analysis presented in

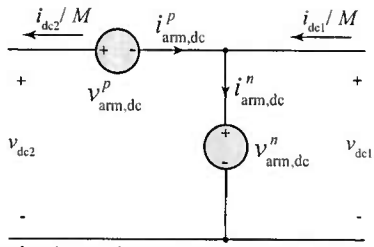
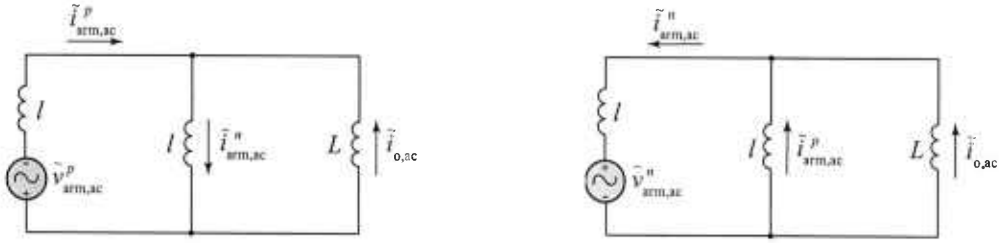


Figure 15: DC equivalent circuit of one phase-leg of the DC MMC.



(a) (b)

Figure 16: AC equivalent circuit of: (a) the upper arm and (b) the lower arm.

this paper, all voltages/currents are represented with respect to the lower arm voltage AC component. Since both DC-link 1 and DC-link 2 terminals of the converter do not carry any AC component under normal operation, for the AC analysis, they can be represented as short circuits. Based on the equivalent circuits of Figs. 16(a) and (b), the following equations are derived for the arm current and phase current AC components:

$$\tilde{i}^p_{arm,ac} = -\frac{\tilde{v}^p_{arm,ac} + \frac{X_L}{X_l+X_L}\tilde{v}^n_{arm,ac}}{j(X_l + \frac{X_lX_L}{X_l+X_L})}, \tag{46}$$

$$\tilde{i}^n_{arm,ac} = -\frac{\tilde{v}^n_{arm,ac} + \frac{X_L}{X_l+X_L}\tilde{v}^p_{arm,ac}}{j(X_l + \frac{X_lX_L}{X_l+X_L})}, \tag{47}$$

$$\tilde{i}_{o,ac} = (\frac{X_l}{X_L + X_l})\frac{\tilde{v}^p_{arm,ac} - \tilde{v}^n_{arm,ac}}{j(X_l + \frac{X_lX_L}{X_l+X_L})}, \tag{48}$$

where X_l is the arm inductive reactance, X_L is the phase inductive reactance.

The arm AC active power can be calculated by:

$$P^x_{arm,ac} = \mathrm{Re}(\tilde{v}^x_{arm,ac}\tilde{i}^{*x}_{arm,ac}), \tag{49}$$

where $\tilde{i}^{*x}_{arm,ac}$ represents the complex conjugate of the upper and lower arm current AC components. By substituting $\tilde{i}^p_{arm,ac}$ from (46) and $\tilde{i}^n_{arm,ac}$ from (47) into (49), the arm AC active power are represented by the following equations:

$$P^p_{arm,ac} = \frac{X_L}{(X_l^2 + 2X_lX_L)}|\tilde{v}^p_{arm,ac}||\tilde{v}^n_{arm,ac}|sin(\phi), \tag{50a}$$

$$P^n_{arm,ac} = -P^p_{arm,ac}, \tag{50b}$$

where ϕ represents the phase angle of the upper arm voltage AC component with respect to lower arm voltage AC component.

Under steady state conditions, to maintain the average voltages of the SM capacitors at their nominal value, the sum of DC and AC active powers of each arm should be equal to zero. By equating the arm DC and AC active powers, the power balance constraint is represented as:

$$(\frac{v_{dc1}}{v_{dc2}} - 1)\frac{P}{M} = -\frac{X_L}{(X_l^2 + 2X_lX_L)}|\tilde{v}^p_{arm,ac}||\tilde{v}^n_{arm,ac}|sin(\phi). \tag{51}$$

2.2 *Converter Design and Component Sizing*

The objective of the component sizing is to minimize the total power losses while satisfying a set of given design constraints. The design constraints include the magnitude of the SM capacitor voltages ripple, total semiconductor power losses, and the amplitude of the AC component of the phase current. The semiconductor power losses, i.e., conduction and switching, mainly depend on the magnitude of the arm current [29]. Since the DC component of the arm current is determined by the operating conditions, the main design goal is to minimize the magnitude of the AC component of the arm current. For this purpose, sizing of the arm and phase filtering inductors as well as the SM capacitor are discussed in this section. In addition to the component sizing, selection of the operating frequency of the converter is also explained. In the following subsections, the operating conditions in Table 4 in Section 2.3.3 are used to demonstrate the design process.

2.2.1 Arm Inductive Reactance

To size the arm inductive reactance, a simplified model is derived and used by assuming that the phase filtering inductive reactance is much larger than the arm inductive reactance ($X_L >> X_l$). Consequently, (46), (47), and (51) are simplified to:

$$\tilde{i}^p_{arm,ac} = \tilde{i}^n_{arm,ac} = -\frac{1}{2jX_l}(\tilde{v}^p_{arm,ac} + \tilde{v}^n_{arm,ac}), \tag{52}$$

$$(\frac{v_{dc1}}{v_{dc2}} - 1)\frac{P}{M} = -\frac{1}{2X_l}|\tilde{v}^p_{arm,ac}||\tilde{v}^n_{arm,ac}|sin(\phi). \tag{53}$$

In the DC-AC MMC used in HVDC applications, the arm reactance serves two main functions: (i) attenuating the high-frequency components of the circulating current and (ii) limiting the DC-side short-circuit fault current. In contrast, in the DC MMC, the AC circulating current is required to exchange active power between the upper and lower arm of each phase-leg, whereby power balance can be maintained within each phase-leg. As a result, the magnitude of the circulating current is controlled to maintain the SM power balance and does not need to be suppressed by passive components. In the DC MMC, the arm inductor acts only as a line impedance such that the voltage across the inductor generates an AC component for the arm current.

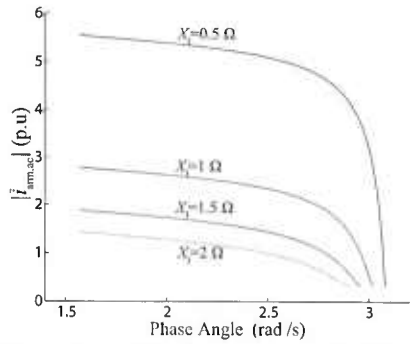


Figure 17: Arm AC current amplitude versus arm voltage phase shifting angle.

Once the DC-link 1 voltage, DC-link 2 voltage, and rated power are given, the amplitude of the arm current AC component can be solved for various phase shifting angle by (52) and (53). The amplitude of the arm AC current versus ϕ for different arm inductive reactance is plotted in Fig. 17. Once the arm inductance is selected, the amplitude of arm current AC component moves along one unique curve shown in Fig. 17 as the phase shifting angle changes from $\pi/2$ to π. As the phase shifting angle approaches π, the amplitude of the arm AC current component reaches a minimum. To minimize the converter losses, the arm AC current amplitude should be minimized by controlling the phase shifting angle and corresponding arm AC voltage amplitude. Based on Fig. 17, the size of arm inductance does not affect the minimum achievable arm current AC component amplitude. However, as the arm inductance decreases, the rate of change of the arm current AC component amplitude with respect to the phase shifting angle increases when the arm current AC component amplitude approaches the minimum value. As a result, a sufficiently large reactance should be selected to ensure that the controller converge to the minimum AC current. Selection of the arm inductance value depends on the controller type/design.

2.2.2 Phase Filtering Inductive Reactance

For proper operation and minimized power losses of the DC MMC, the AC component of the output phase current should be negligible. This necessitates a large phase filtering inductive reactance, which for high power/voltage applications, adds to the system cost and complexity. Therefore, it is of interest to determine the minimum phase filtering inductive reactance that satisfies the constraint on the amplitude of AC current component of the phase current. The amplitude of the phase AC current can be determined by solving (48) for various phase filtering inductive reactances. Fig. 18 shows the amplitude of the AC component of the phase current versus the phase filtering inductive reactance. As the phase inductive reactance increases, the current amplitude decreases. However, the rate of change of the phase current AC component is reduced as the phase inductance increases, which means the marginal cost of reducing the phase current AC component is increased. A minimum phase inductance can be identified to keep the phase current amplitude below a certain value given as a design constraint.

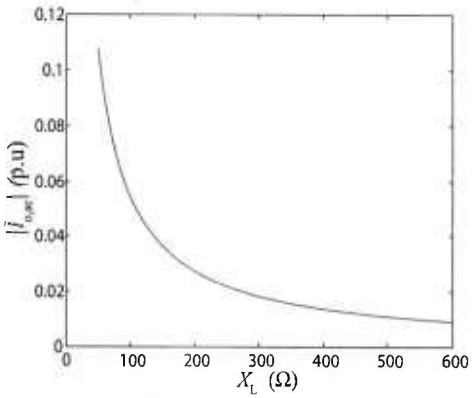


Figure 18: Phase AC current amplitude versus phase filtering inductive reactance.

2.2.3 SM Capacitive Reactance

The SM capacitive reactance is determined based on the magnitude of its voltage ripple. A smaller capacitive reactance leads to a lower SM voltage ripple amplitude but higher cost. The design objective for the SM capacitive reactance is to identify the maximum SM reactance that satisfies the SM capacitor voltage ripple constraint.

The dynamic of the sum of the SM capacitor voltages can be expressed by [30] :

$$\frac{\mathrm{d}v^{\Sigma p,n}}{\mathrm{d}t} = \frac{N}{Cv_{\mathrm{dc2}}} v_{\mathrm{arm}}^{p,n} i_{\mathrm{arm}}^{p,n}, \tag{54}$$

where C is the SM capacitance and $v^{\Sigma p,n}$ is the sum of SM capacitor voltages of the upper or lower arm. The sum of the SM capacitor voltages is given by:

$$v^{\Sigma p,n} = Nv_{C,\mathrm{nominal}} + N\Delta v_C^{p,n}, \tag{55}$$

where $v_{C,\mathrm{nominal}}$ represents the nominal value of the SM capacitor voltage and $\Delta v_C^{p,n}$ represents the ripple component of the SM capacitor voltage of the upper or lower arm.

The arm voltages can be expressed by:

$$v_{\mathrm{arm}}^{p} = (v_{\mathrm{dc2}} - v_{\mathrm{dc1}}) + V_p \cos(\omega t + \phi), \tag{56}$$

$$v_{\mathrm{arm}}^{n} = v_{\mathrm{dc1}} + V_n \cos(\omega t), \tag{57}$$

where V_p and V_n represent the amplitude of the AC component of the upper and lower arms, respectively, and ω represents the converter operating frequency.

The arm currents can be expressed by:

$$i_{\mathrm{arm}}^{p} = -\frac{i_{\mathrm{dc2}}}{M} + I_p \cos(\omega t + \phi_p), \tag{58}$$

$$i_{\mathrm{arm}}^{n} = \frac{i_{\mathrm{dc2}}}{M}\left(\frac{v_{\mathrm{dc2}}}{v_{\mathrm{dc1}}} - 1\right) + I_n \cos(\omega t + \phi_n), \tag{59}$$

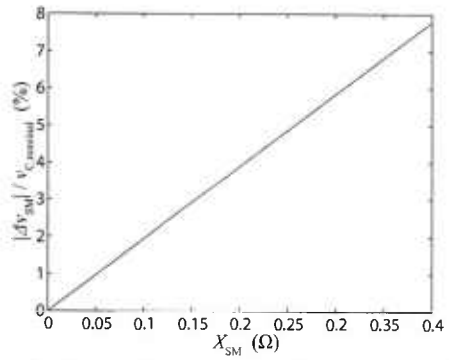


Figure 19: The normalized magnitude of the SM capacitor voltage ripple versus the SM capacitive reactance.

where ϕ_p and ϕ_n represent the phase angle of the AC component of the upper and lower arm currents with respect to the lower arm voltage, respectively, and I_p and I_n represent the amplitude of the upper and lower arm current AC component, respectively.

Substituting for $\tilde{v}^{p,n}_{\text{arm,ac}}$ and $\tilde{i}^{p,n}_{\text{arm,ac}}$ from (56)-(59) to (54) and integrating both sides of the results, the SM capacitor voltage ripple component can be expressed by:

$$\Delta v_C^p = (1 - \frac{v_{\text{dc1}}}{v_{\text{dc2}}})\frac{I_p}{\omega C}\sin(\omega t + \phi_p) - \frac{V_p i_{\text{dc2}}}{M v_{\text{dc2}}\omega C}\sin(\omega t + \phi) + \frac{I_p V_p}{4 V_{\text{dc2}}\omega C}\sin(2\omega t + \phi + \phi_p), \quad (60)$$

$$\Delta v_C^n = \frac{v_{\text{dc1}} I_n}{v_{\text{dc2}}\omega C}\sin(\omega t + \phi_n) + (\frac{v_{\text{d2}}}{v_{\text{d1}}} - 1)\frac{V_n i_{\text{dc2}}}{M v_{\text{dc2}}\omega C}\sin(\omega t) + \frac{I_n V_n}{4 V_{\text{dc2}}\omega C}\sin(2\omega t + \phi_n). \quad (61)$$

As shown in (60) and (61), the capacitor voltages of the SMs in the upper and lower arms contain one fundamental component term as well as a second-order harmonic term. The amplitude of the fundamental term depends upon the ratio of the input and output DC-link voltages. The SM capacitor voltages in the upper and lower arms have the same ripple magnitude only if the ratio of v_{dc1} and v_{dc2} is 0.5. Therefore, while evaluating the SM capacitor voltage ripple, the larger value of the SM capacitor voltage ripple magnitude between the upper and lower arms is considered to select the SM capacitive reactance. Solving (60) and (61), the normalized magnitude of the SM capacitor voltage ripple versus the SM capacitive reactance is shown in Fig. 19 for $v_{\text{dc1}}/v_{\text{dc2}} = 0.5$. Based on Fig. 19, the maximum SM capacitive reactance can be determined to satisfy the SM capacitor voltage ripple requirement.

2.2.4 Operating Frequency

Unlike the DC-AC MMC used in the HVDC applications in which the operating frequency is imposed by the converter AC-side frequency, the operating frequency of the

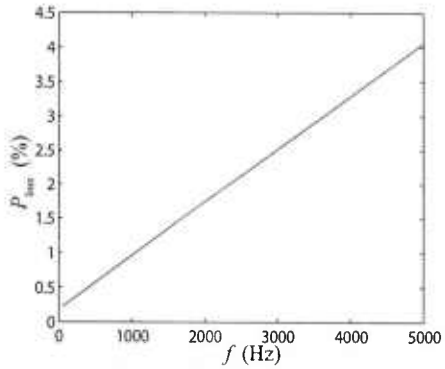


Figure 20: Converter semiconductor device losses versus the operating frequency.

DC MMC is a free design parameter. The operating frequency can be chosen based on a trade-off between the component size/cost and the converter efficiency. To choose a proper AC operating frequency, the power losses of the converter are evaluated at various operating frequencies. Since a higher operating frequency leads to smaller passive components size/cost, the maximum AC operating frequency that satisfies the power loss constraint is identified. Since the semiconductor devices make the major contribution to the converter total power losses [31], the power loss constraint is set for semiconductor devices losses. To calculate the power losses, a power loss estimation method based on semiconductor behavior model is adopted from [32,33]. By applying this method, the total conduction and switching losses of the DC MMC at the given operating condition are evaluated for various operating frequencies. The converter total semiconductor device losses versus the converter operating frequency are shown in Fig. 20. Once the operating frequency is chosen, the arm and phase filtering inductances as well as the SM capacitance can be determined based on the operating frequency and their corresponding reactances, determined in the previous steps.

The procedure to size the components of the DC MMC is illustrated in the flowchart of Fig. 21. Given the nominal operating conditions and the design constraints, first, the arm inductive reactance is selected based on the controller design. The arm inductive reactance should be sized to guarantee that the controller converges to the achievable minimum arm AC current. As shown in Fig. 21, several iterations might be required to find the set of components, which satisfy the design constraints. Once an arm reactance is selected, the amplitude of the AC component of the phase current is calculated for various phase filtering inductive reactances. A minimum phase filtering reactance that satisfies the phase current AC component amplitude constraint can be identified in this step. The SM capacitor voltage ripple magnitude will then be calculated for different SM capacitive reactances. A maximum SM capacitive reactance will be identified to satisfy the constraint on the SM voltage ripple magnitude. In the next step, semiconductor power losses are estimated at various frequencies and the maximum frequency that satisfies the power loss constraint can then be identified. After this step, the controller performance will be evaluated by simulation studies. If the controller fails to converge, the arm inductive reactance will be resized. If the controller performance is satisfied, the arm and output inductors as well as the SM

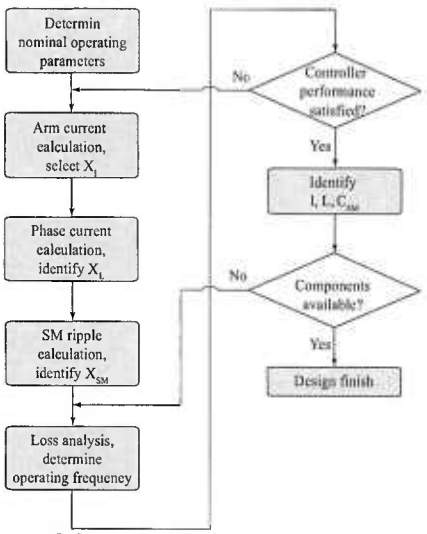


Figure 21: Flowchart of the component sizing procedure of the DC MMC.

capacitor can be sized.

2.2.5 Simulation Results

Simulation results are reported in this section on a three-phase-leg DC MMC, using parameters and corresponding constraints listed in Tables 4. The studies are conducted to validate the developed steady state model and demonstrate the accuracy of the converter design process. The sizes of the passive components are determined based on the design procedure proposed in Section 2.2. Two modes of operations are simulated to mimic the bidirectional power flow: the buck mode of operation, which is defined as DC power flowing from the DC-link 2 to the DC-link 1 and the boost mode of operation, which is defined as DC power flowing from the DC-link 1 to the DC-link 2. The designed converters are simulated in the PSCAD/EMTDC software environment. The sinusoidal pulse width modulation (SPWM) scheme in conjunction with the open-loop control strategy in [34] are used in the simulation studies. The steady state converter waveforms for buck and boost modes of operation of the DC MMC are provided in Figs. 22 and 23, respectively, where $v_{dc1}/v_{dc2} = 0.5$. In both figures, the SM capacitor voltages and arm currents of only the phase-*a* are shown. The nominal conditions, design constraints, converter parameters, and analytical results are shown in Table 4. By following the described design procedure, an arm reactance of 2 Ω is selected to ensure the convergence of the controller. An output reactance of 450 Ω is chosen, which results in 9.8 A phase AC current amplitude. X_{SM} is selected as 0.2 Ω, which results in 3.8% SM capacitor voltage ripple. An AC operating frequency of 360 Hz is chosen, leading to 0.5% semiconductor power losses.

Since $v_{dc1}/v_{dc2} = 0.5$, the DC components of i^p_{arm} and i^n_{arm} have the same magnitude as shown in Figs. 22(c) and 23(c). The magnitudes of the SM capacitor voltages ripple in the upper and lower arms are almost the same, i.e., 74 V for buck mode of operation and 78 V for boost mode of operation. The peak to peak magnitude of the AC component of the phase current is equal to 18 A for both modes of operation. As confirmed by the waveforms

Table 4: Nominal conditions and design constraints of the study system

Nominal Conditions	**Value**
Rated converter power, P	7 MW
DC-link 1 voltage, v_{dc1}	8.8 kV
DC-link 2 voltage, v_{dc2}	4.4 kV
Design Constraints	**Value**
Phase current ripple, $\lvert\tilde{i}_{o,ac,p\text{-}p}\rvert/i_{o,dc}$	5%
SM voltage ripple, $\lvert\Delta v_{SM}\rvert/v_{C,nominal}$	4%
Converter power losses	1%
Converter Parameters	**Value**
Number of SMs per arm, N	4
SM capacitor, C_{SM}	2 mF
Arm inductor, l	0.89 mH
Phase filtering inductor, L	132 mH
Operating frequency, f	360 Hz
Performance Parameters	**Analytical Results**
Phase current ripple, $\lvert\tilde{i}_{o,ac,p\text{-}p}\rvert$	19.6 A
SM capacitor voltage ripple $\lvert\Delta v_{SM}\rvert$	81.6 V
Converter power losses	0.5%

of Figs. 22 and 23, the magnitude of the SM capacitor voltages ripple and AC component of the phase current are below the design constraints for both modes of operation.

2.3 Closed-loop Control of the DC MMC

In the DC MMC, the power flow within each arm can be decomposed into a DC and an AC component. The DC power component is controlled to transfer the commanded power between the input and output DC links. An AC circulating current needs to be injected and controlled to exchange active AC power between the upper and lower arms of each phase-leg such that the power balance of each SM capacitor is maintained. The arm AC active power should be actively controlled to follow the arm DC power in the upper and lower arms by controlling $\tilde{v}^p_{arm,ac}$ and $\tilde{v}^n_{arm,ac}$. As shown in (51) there are infinite possible combinations of control inputs, i.e., $\tilde{v}^p_{arm,ac}$ and $\tilde{v}^n_{arm,ac}$, that satisfy the power balance constraints. However, from the power loss and device rating perspectives, the amplitude of AC circulating current must be minimized. To minimize the AC circulating current that delivers a constant amount of arm AC power, the amplitudes of the AC components of the arm voltages must be maximized.

To minimize the divergence between the SM capacitor voltages of the upper and lower arms, a closed-loop control strategy is required. The closed-loop control strategy for the DC MMC involves three tasks: (i) minimization of the voltage divergence between the SM capacitors of the upper and lower arms; (ii) minimization of the circulating current required to exchange active AC power; and (iii) regulation of the output DC-link voltage. To this end, two closed-loop control strategies are proposed in this section: an MCC, which

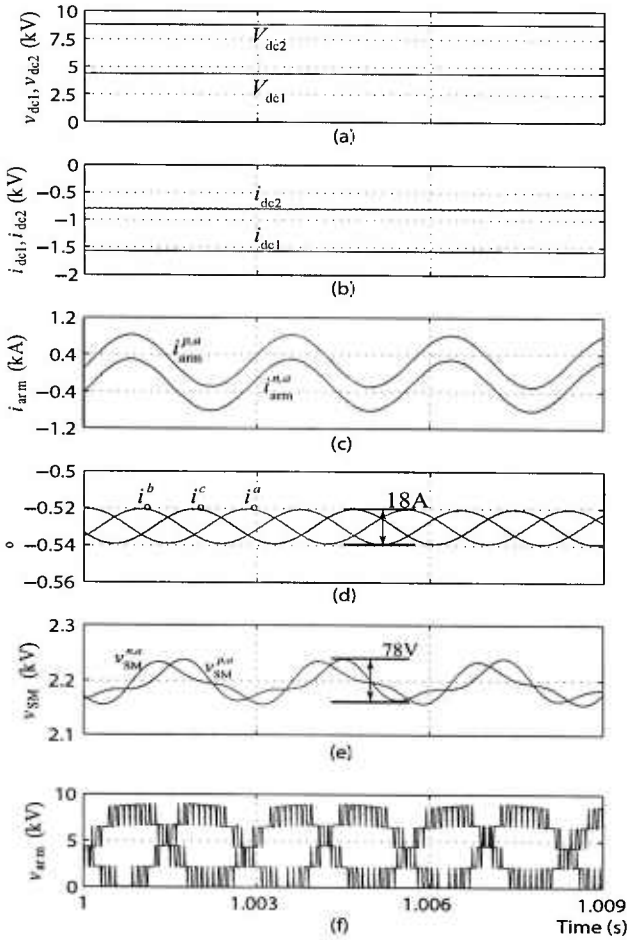


Figure 22: Steady-state converter waveforms for buck mode of operation for v_{dc1}/v_{dc2} = 0.5: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-*a*, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-*a* and (f) upper and lower arm voltages of phase-*a*.

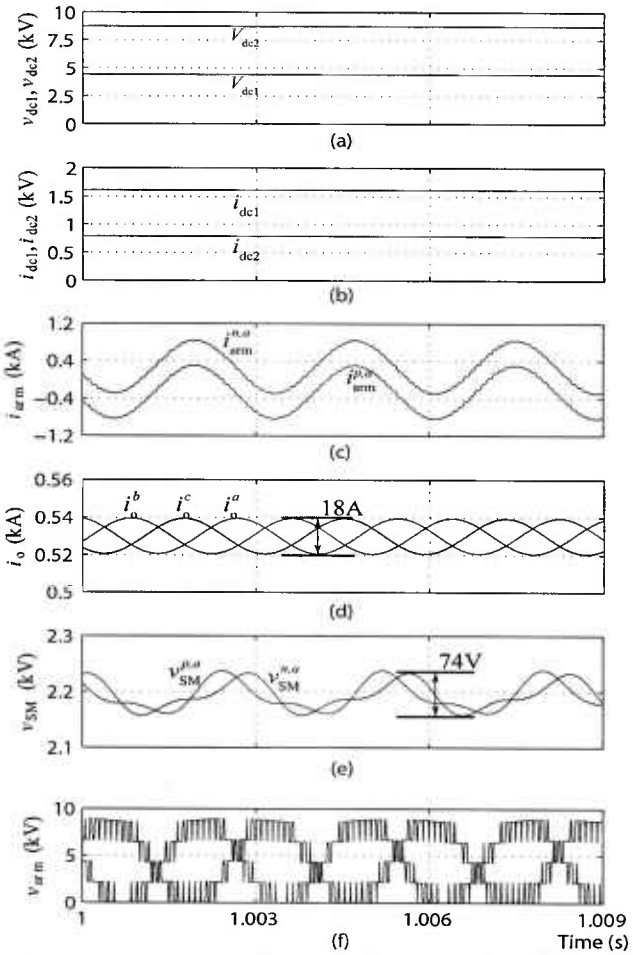


Figure 23: Steady-state converter waveforms for boost mode of operation for v_{dc1}/v_{dc2} = 0.5: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-*a*, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-*a* and (f) upper and lower arm voltages of phase-*a*.

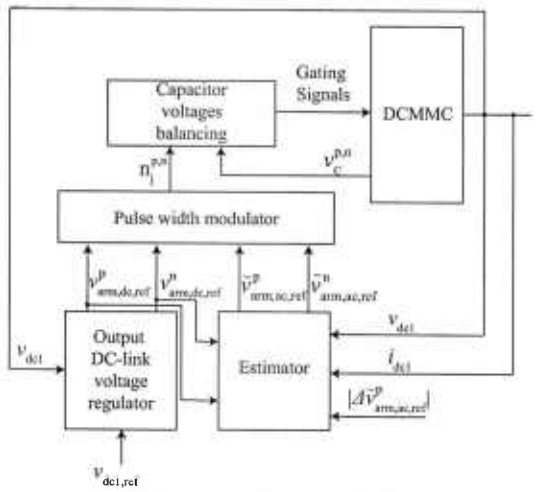


Figure 24: Overall block diagram of the proposed MCC.

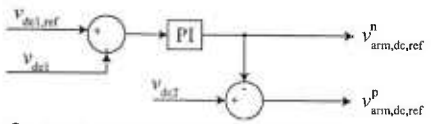


Figure 25: Output voltage regulator of the proposed MCC.

is based on the phasor-domain model of the DC MMC, and a PCC, which is based on an perturb and observe algorithm.

2.3.1 The MCC

Fig. 24 shows overall block diagram of the proposed MCC. The MCC consists of an outer loop to regulate the output DC-link voltage combined with an inner loop to maintain the SM capacitor voltages balanced. In this control strategy, the SM capacitor voltages of the upper and lower arms and the output DC-link voltage and current are the measured variables. The upper and lower arm voltage references are the outcomes of the closed-loop control.

Block diagram of the output voltage regulator of the MCC is shown in Fig. 25. To regulate the output DC-link voltage at its reference value, the outer loop employs a Proportional-Integral (PI) controller that acts on the difference between the reference and measured output DC-link voltage to generate the reference value for the DC component of the lower arm voltage, $v^{n}_{arm,dc,ref}$. The reference value for the DC component of the upper arm voltage, $v^{p}_{arm,dc,ref}$, is determined by subtracting $v^{n}_{arm,dc,ref}$ from v_{dc2} to satisfy the KVL in the DC loop formed by v_{dc2}, $v^{p}_{arm,dc}$ and $v^{n}_{arm,dc}$.

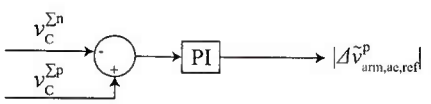


Figure 26: Auxiliary controller of the proposed MCC.

To maintain the power balance between the upper and lower arms, an estimator shown in Fig. 24 is used to generate the reference amplitude for the AC components of the upper and lower arm voltages, $|\tilde{v}^{p}_{\text{arm,ac,ref}}|$ and $|\tilde{v}^{n}_{\text{arm,ac,ref}}|$, respectively, as well as the reference phase angle for the AC component of the upper arm voltage, ϕ_{ref}. $|\tilde{v}^{n}_{\text{arm,ac,ref}}|$ is maintained at its maximum value while $|\tilde{v}^{p}_{\text{arm,ac,ref}}|$ is controlled by the estimator to regulate the AC active power exchange. First, the required arm AC active power to maintain the power balance between the upper and lower arms is determined by substituting for the measured DC-link voltages and current in (45). To minimize the AC circulating current, $|\tilde{v}^{p}_{\text{arm,ac}}|_{\max}$ should be applied as the reference. $|\tilde{v}^{p}_{\text{arm,ac}}|_{\max}$ and $|\tilde{v}^{n}_{\text{arm,ac}}|_{\max}$ are then determined by substituting for $v^{p}_{\text{arm,dc,ref}}$ and $v^{n}_{\text{arm,dc,ref}}$, which are generated by the outer control loop into (39) and (40). Finally, ϕ_{ref} is determined by substituting for the measured DC-link voltages, P, $|\tilde{v}^{p}_{\text{arm,ac,ref}}|$, and $|\tilde{v}^{n}_{\text{arm,ac,ref}}|$ into (51).

Assuming equal power sharing among M phase-legs, the estimator uses the measured P to estimate the reference signals that minimize the AC circulating current for each phase-leg. This assumption is valid under normal operating conditions. To improve the accuracy and robustness of the MCC to minimize the AC circulating current, the output power of each phase-leg can be measured by measuring the output current of each phase-leg and used to determine the reference signals. This approach, however, will adds to the cost and complexity of the converter for high-power applications, where multiple phase-legs need to be installed.

For the sake of disturbance rejection, a compensating signal, $|\Delta\tilde{v}^{p}_{\text{arm,ac,ref}}|$, is generated by an auxiliary controller shown in Fig. 26. The auxiliary controller employs a PI controller acting on the difference between the sum of the SM capacitor voltages of the upper and lower arms to correct steady state error of the SM capacitor voltage balancing and to assist the estimator in maintaining the power balance during converter start-up and transients. The compensating signal is added to $|\tilde{v}^{p}_{\text{arm,ac,ref}}|$, which is generated by the estimator.

2.3.2 The PCC

The block diagram of the proposed PCC is shown in Fig. 27. Similar to the MCC, the PCC has an outer loop, which regulates the output DC-link voltage combined with an inner loop, which maintains the SM capacitor voltages between the upper and lower arms balanced. Nevertheless, the PCC requires less measured variables as the output DC-link voltage and the SM capacitor voltages of the upper and lower arms are the only variables to be measured.

The outer loop voltage controller has the same structure as the one in the MCC. In this section, the inner loop power balance control will be explained. To explain the operation of the PCC, two error signals are defined:

$$e_1 = |\tilde{v}^{p}_{\text{arm,ac}}|_{\max} - |\tilde{v}^{p}_{\text{arm,ac,ref}}|, \tag{62}$$

$$e_2 = v_C^{\Sigma p} - v_C^{\Sigma n}, \tag{63}$$

where $v_C^{\Sigma p}$ and $v_C^{\Sigma n}$ represent the sum of the SM capacitor voltages of upper and lower arms, respectively.

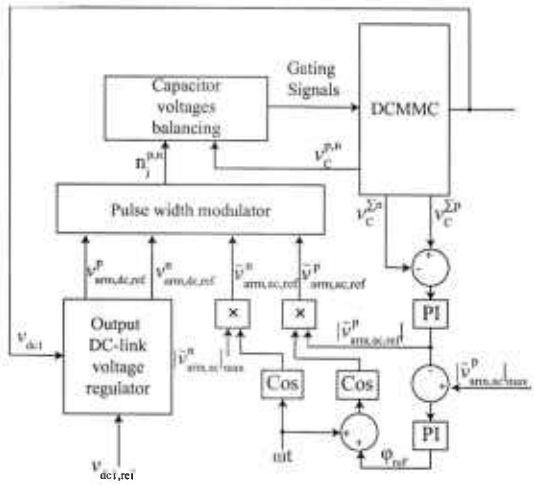


Figure 27: Overall block diagram of the proposed PCC.

The inner loop of the PCC consists of two PI controllers acting on e_1 and e_2. $|\tilde{v}^n_{arm,ac}|$ is fixed at its maximum value determined by (40) and $|\tilde{v}^p_{arm,ac}|$ and ϕ are the outcomes of the closed-loop control. Deviation of e_1 from zero indicates power imbalance between the upper and lower arms such that the sum of the SM capacitor voltages diverges from the lower one. The PI controller adjusts $|\tilde{v}^p_{arm,ac,ref}|$ to correct the power imbalance between the upper and lower arms. If $e_2 > 0$, which indicates $|\tilde{v}^p_{arm,ac,ref}|$ is smaller than its maximum available value, the PI controller increases ϕ. As ϕ increases, the required $|\tilde{v}^p_{arm,ac,ref}|$ to establish power balance between the upper and lower arms is increased, which leads to an increasing in e_1. The PI controller that acts on e_1 will increase $|\tilde{v}^p_{arm,ac,ref}|$ to reduce the divergence between the sum of the SM capacitor voltages of the upper and lower arms until $|\tilde{v}^p_{arm,ac,ref}|$ reaches its maximum attainable value, $|\tilde{v}^p_{arm,ac}|_{max}$. If $e_2 < 0$, meaning that $|\tilde{v}^p_{arm,ac,ref}|$ is greater than its maximum value and the converter operates in over-modulation mode, the PI controller acting on e_2 decreases ϕ. As ϕ deceases, e_1 becomes negative since $|\tilde{v}^p_{arm,ac,ref}|$ required to establish power balance between the upper and lower arms is reduced. The PI controller that acts on e_1 will decrease $|\tilde{v}^p_{arm,ac,ref}|$ to minimize the divergence between the sum SM capacitor voltages of the upper and lower arms until $|\tilde{v}^p_{arm,ac,ref}|$ drops to its maximum attainable value.

Since the push-pull operation ensures that $|\tilde{v}^p_{arm,ac}|$ and $|\tilde{v}^n_{arm,ac}|$ operate at their maximum attainable values, the AC circulating current is minimized. In addition, the divergence between the sum of SM capacitor voltages of the upper and lower arms is minimized.

2.3.3 Simulation Results

To demonstrate performance and effectiveness of the proposed control strategies, a two-phase-leg DC MMC is simulated in the PSCAD/EMTDC software environment. The system parameters and operating conditions are listed in Table 5. Although the DC MMC is capable of bidirectional power transfer, without loss of generality, buck mode of operation, i.e., DC power flowing from the DC-link 2 to the DC-link 1, is considered for simulation studies.

Table 5: Parameters of the study system

Converter Parameters	Value
Number of phase-legs, M	2
Number of SMs per arm, N	4
SM capacitor, C_{SM}	2.6 mF
Arm inductor, l	1.1 mH
Phase filtering inductor, L	210 mH
Operating frequency, ω	360 Hz
Rated Power, P	7 MW
DC-link 2 voltage, v_{dc2}	8.8 kV

The DC MMC operating with each of the proposed control strategies is simulated under two scenarios. In Scenario I, the DC MMC operates in buck mode of operation with a reference output DC-link voltage of 4.4 kV. Initially, the converter transfers 3.5 MW power (half load). At t = 0.5 s, the output power is ramped up from 3.5 MW to 7 MW (full load). In Scenario II, the DC MMC operates in buck mode of operation with an reference output DC-link voltage of 4.4 kV transferring 4.86 MW power. At t = 0.5 s, the reference output DC-link voltage is ramped up from 4.4 kV to 5.28 kV (10% increase), which corresponds to ramping the transfered power from 4.68 MW to 7 MW (full load).

2.3.3.1 Simulation Results under the MCC

The simulated waveforms for the study system based on the MCC in Scenario I are shown in Figs. 28 and 29. Initially, the DC MMC system of Fig. 13 is in a steady state condition and 3.5 MW power is flowing from the DC-link 2 to the DC-link 1. $v_{dc1,ref}$ is set to 4.4 kV. At t = 0.5 s, the output power is ramped up to 7 MW. Figs. 28(a) and (b) show the DC-link voltages and currents of the DC MMC phase-a, respectively. As depicted, the DC-link 1 voltage is well regulated at 4.4 kV under both transient and steady state conditions. As shown in Fig. 28(d), the SM capacitor voltages are maintained at their nominal value of 2.2 kV. The magnified waveforms during and subsequent to the ramp-up are shown in Fig. 29. Since the converter operates with a duty ratio of 0.5, the maximum amplitude of the AC component of the arm voltage is 4.4 kV. As shown in Figs. 29(b) and (d), the AC components of the arm voltages are maintained at the vicinity of their maximum value during ramp-up and steady state. As a result, the AC circulating current is maintained at its minimum value. Moreover, as shown in Figs. 29(a) and (c), the divergence between the SM capacitor voltages of the upper and lower arms are minimized.

The simulated waveforms for the study system based on MCC in Scenario II are provided in Figs. 30 and 31. Initially, the DC MMC system of Fig. 13 is in a steady state condition and 4.86 MW power is flowing from the DC-link 2 to the DC-link 1. $v_{dc1,ref}$ is set to 4.4 kV. At t = 0.5 s, $v_{dc1,ref}$ is ramped up by 10% to 5.28 kV, corresponding to power ramp-up from 4.86 MW to 7 MW. As shown in Fig. 30(a), subsequent to the ramp, the output DC-link voltage is well regulated at 5.28 kV. As the output DC-link voltage increases from 4.4 kV to 5.28 kV, the DC component of the lower arm voltage shown in Fig. 31(d) is

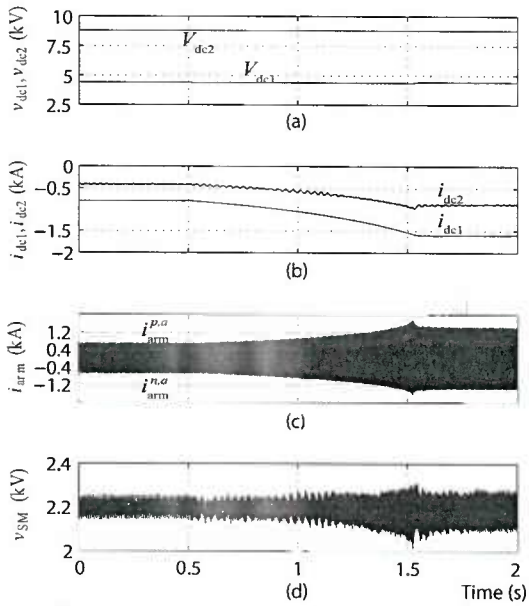


Figure 28: Converter waveforms in Scenario I with the MCC: (a) input and output DC-link voltages, (b) input and output DC-link current, (c) upper and lower arm currents of phase-*a*, and (d) SM capacitor voltages of the upper and lower arms of phase-*a*.

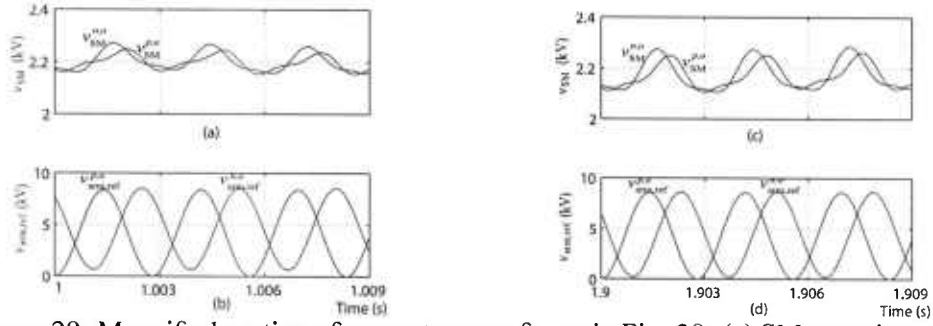


Figure 29: Magnified portion of converter waveforms in Fig. 28: (a) SM capacitor voltages of the upper and lower arms of phase-*a*, (b) reference AC voltages of the upper and lower arms of phase-*a*, (c) SM capacitor voltages of the upper and lower arms of phase-*a*, and (d) reference AC voltages of the upper and lower arms of phase-*a*.

increased while that of the upper arm voltage is decreased. As a result, the maximum amplitudes of the AC component of both the upper and lower arms are decreased. Subsequent to the ramp-up transient, the AC components of the arm voltages are maintained at their maximum value. Furthermore, the SM capacitor voltages are maintained balanced under both transient and steady state conditions, as shown in Fig. 31.

2.3.3.2 Simulation Results under the PCC

The simulated waveforms for the study system based on the PCC in Scenario I are shown in Figs. 32 and 33. The output DC-link voltage is regulated at 4.4 kV and the SM

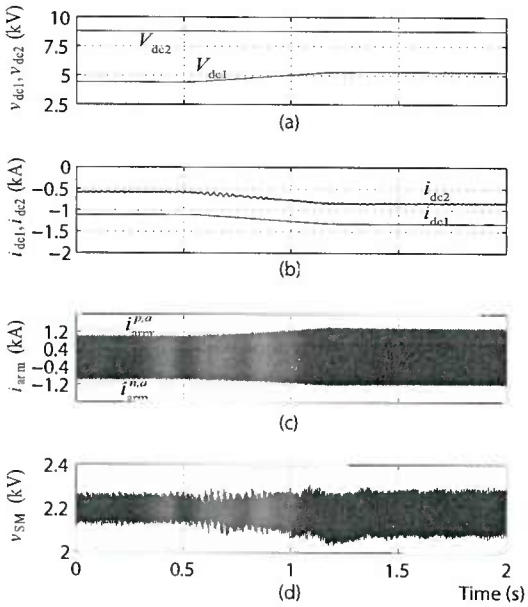


Figure 30: Converter waveforms in Scenario II with the MCC: (a) input and output DC-link voltages, (b) input and output DC-link currents, (c) upper and lower arm currents of phase-*a*, and (d) SM capacitor voltages of the upper and lower arms of phase-*a*.

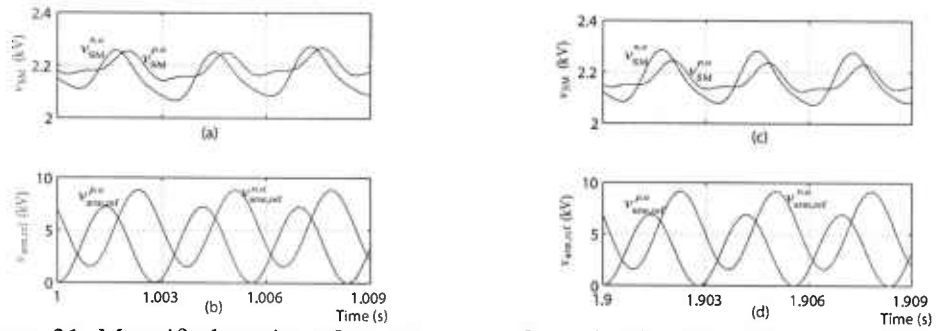


Figure 31: Magnified portion of converter waveforms in Fig. 30: (a) SM capacitor voltages of the upper and lower arms of phase-*a*, (b) reference AC voltages of the upper and lower arms of phase-*a*, (c) SM capacitor voltages of the upper and lower arms of phase-*a*, and (d) reference AC voltages of the upper and lower arms of phase-*a*.

capacitor voltages are maintained balanced under both steady state and transient conditions. In addition, the AC components of the arm voltages are maintained at their maximum value as shown in Figs. 33(b) and (d). As confirmed by the simulation results, both the MCC and PCC are capable of simultaneously regulating the output DC-link voltage, maintaining the SM capacitor voltages balanced and minimizing the AC circulating current.

The corresponding simulated waveforms based on the PCC in Scenario II are shown in Figs. 34 and 35. As confirmed by the waveforms, the PCC is capable of regulating the output DC-link voltage, maintaining the SM capacitor voltages balanced, and minimizing the circulating current under both transient and steady state conditions.

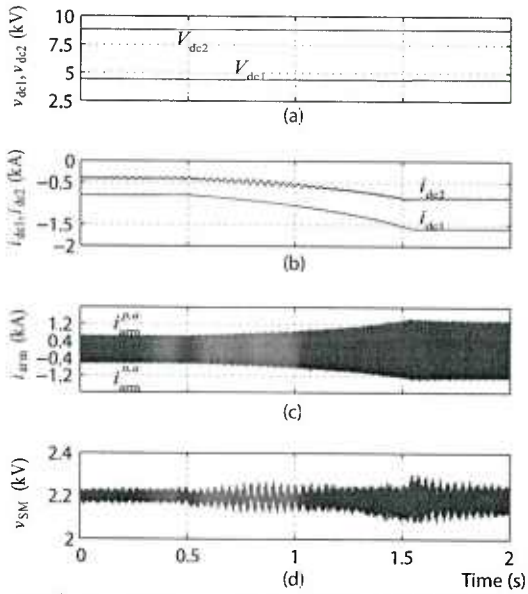


Figure 32: Converter waveforms in Scenario I with the PCC: (a) input and output DC-link voltages, (b) input and output DC-link current, (c) upper and lower arm currents of phase-*a*, and (d) SM capacitor voltages of the upper and lower arms of phase-*a*.

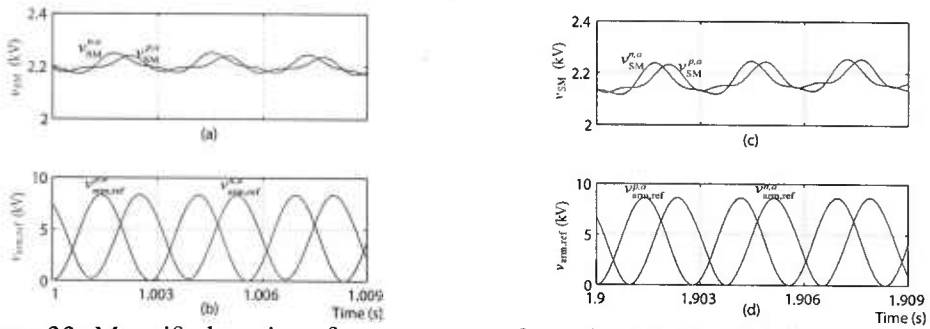


Figure 33: Magnified portion of converter waveforms in Fig. 32: (a) SM capacitor voltages of the upper and lower arms of phase-*a*, (b) reference AC voltages of the upper and lower arms of phase-*a*, (c) SM capacitor voltages of the upper and lower arms of phase-*a*, and (d) reference AC voltages of the upper and lower arms of phase-*a*.

2.4 *Conclusions*

In this chapter, a phasor-domain steady state mathematical model for the DC MMC is proposed. Based on the proposed model, a systematic procedure of sizing the converter components is developed. Proper sizing of the components ensures the converter achieve high efficiency while satisfying a set of given design requirements. Two closed-loop control strategies, one based on an MCC and the other based on a PCC are proposed to simultaneously regulate the output DC-link voltage, maintain the SM capacitor power balanced, and minimize the AC circulating current of the DC MMC. Simulation results are presented to demonstrate the accuracy of the proposed design procedure as well as the effectiveness of

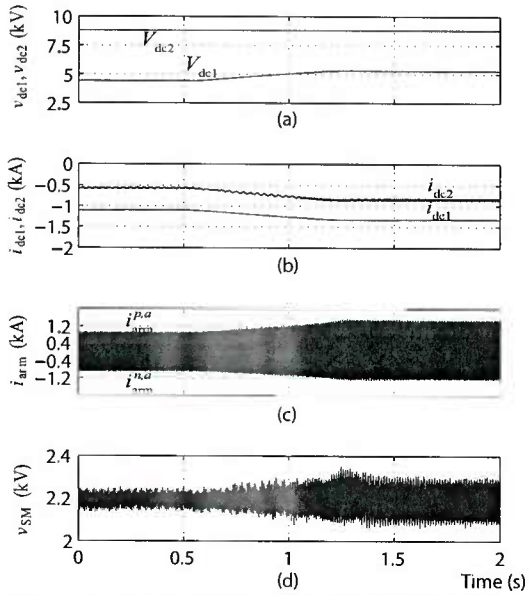


Figure 34: Converter waveforms in scenario II with PCC: (a) input and output DC-link voltages, (b) input and output DC-link current, (c) upper and lower arm currents of phase-a, and (d) SM capacitor voltages of the upper and lower arm of phase-*a*.

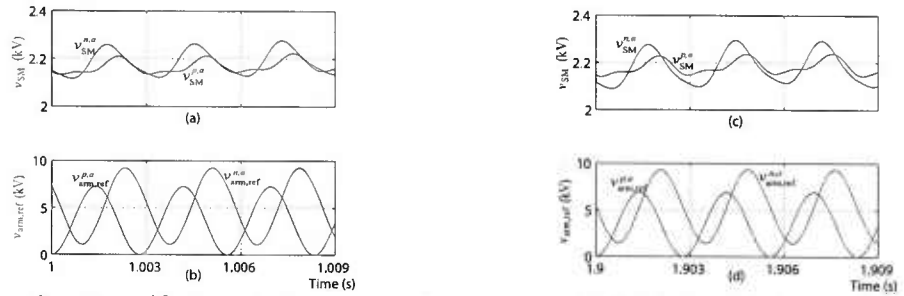


Figure 35: Magnified portion of converter waveforms in Fig. 34: (a) SM capacitor voltages of the upper and lower arms of phase-*a*, (b) reference AC voltages of the upper and lower arms of phase-*a*, (c) SM capacitor voltages of the upper and lower arms of phase-*a*, and (d) reference AC voltages of the upper and lower arms of phase-*a*.

the proposed control strategies.

PUBLICATIONS UNDER THIS GRANT

- S. Debnath, J. Qin, and M. Saeedifard, "Control and Stability Analysis of Modular Multilevel Converter Under Low-Frequency Operation," IEEE Tran. Ind. Electro., vol. 62, no. 9, pp. 5329-5339, 2015.
- S. Debnath, M. Saeedifard, "Simulation-based Gradient-Descent Optimization of Modular Multilevel Converter Controller Parameters," IEEE Tran. Ind. Electro., no. 99, pp. 1, 2015.
- H. Yang, J. Qin, S. Debnath, M. Saeedifard, "Phasor-Domain Steady-State Modeling and Design of the DC-DC Modular Multilevel Converter," submitted to IEEE Trans. Power Del., under review 2015.
- H. Yang, M. Saeedifard, "Closed-loop Control of the DC-DC Modular Multilevel Converter," submitted to IEEE Trans. Power Del., under review 2015.

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